ISSN 0735-2727, Radioelectronics and Communications Systems, 2022, Vol. 65, No. 7, pp. 365–375. © Allerton Press, Inc., 2022.
Russian Text © The Author(s), 2022, published in Izvestiya Vysshikh Uchebnykh Zavedenii, Radioelektronika, 2022, Vol. 65, No. 7, pp. 433–444.

Structural and Parametric Optimization of Bandgap Voltage Reference

L. N. Pavlov[1*] and D. Yu. Lebedev[1]**

[1]*National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute", Kyiv, Ukraine*
**ORCID: 0000-0001-8273-9607, e-mail: leonpavl@gmail.com*
***ORCID: 0000-0001-8672-8366, e-mail: d.lebedev@kpi.ua*

Received December 1, 2021
Revised May 16, 2022
Accepted June 20, 2022

Abstract—The article shows the possibility of reducing the temperature coefficient for the bandgap voltage reference (BVR) built on bipolar transistors. To do this, as the first step, it is proposed to divide the temperature range of BVR operation into two intervals. Since the most probable working interval corresponds to the range of positive temperatures, such division makes it possible to halve the temperature coefficient for the most probable working area on condition of an appropriate BVR adjustment. The introduction of weights for BVR optimization involves giving preference to the working interval of positive temperatures. It provides a direction of search for the optimal solution when formalizing the optimization process. The second step involves the proposal of a functional block diagram with compensators of the decline of temperature characteristic. The paper also proposes electric circuits of a typical compensator and the circuits for connecting one and two compensators to uncompensated BVR. This also determines the rule of introducing further compensators, if expedient. The parametric optimization of the proposed BVR circuits and the experimental study of BVR circuit with one compensation link have been performed. The above optimization resulted in a reduced value of temperature coefficient at the level of 2.88 ppm/°C for the circuit with one compensator and 1.0 ppm/°C for the case of connecting two compensators to BVR circuit that surpasses the latest published achievements. When expanding the temperature range into the area of low temperatures and using additional compensators in accordance with the specified schematic block diagram, we could expect the reduction of the temperature coefficient to 0.25–0.5 ppm/°C.

DOI: 10.3103/S0735272722070056

1. INTRODUCTION

The subject of this study deals with the class of bandgap voltage references (BVR) that are based on theoretical principles of forbidden zone. Such BVR occupy a special place both as an independent integrated circuit and as an important assembly in a sizable list of integrated circuit nomenclature: analog-digital and digital-analog converters, secondary power supply sources, DC/DC converters, etc.

The architecture of these BVR usually contains the voltage source that is proportional to absolute temperature (PTAT) and the voltage source that is complementary to absolute temperature (CTAT). The specified PTAT and CTAT sources, usually, compensate one another for obtaining the constant output voltage only at one point of the temperature range. As the temperature fluctuates with respect to the design point, the reference voltage changes and a magnitude of this change generally increases with the increasing temperature deviation.

2. PROBLEM STATEMENT

This study is aimed at reducing the nonlinearity of BVR temperature characteristic in the most probable area of working temperature. Indeed, the equipment is operated most often under the normal weather conditions or under conditions of elevated environmental temperature.

Since the case, when the working temperature is below 0 °C, most often corresponds only at the beginning of operation of radio technical equipment or devices in conditions of negative temperatures. Hence, the following tasks should be solved for achieving the specified aim:

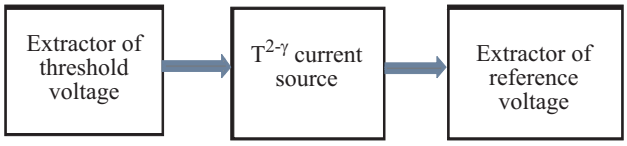

Fig. 1. Precision BVR.

1. To carry out the structuring of input data as the first step of optimization: to divide the temperature range into two areas and assign them weight factors that will be taken into account in a formalized search for optimal solution.

The first domain is the apparatus switching on area that lies in the region of sub-zero temperatures. In this region, requirements to BVR can be significantly weakened. The weight factor can be 5 times as small as in the most probable temperature domain of BVR operation in the region of positive temperatures. This will enable us to formalize the process of future optimization in order to minimize the instability boundaries in the most required working range, where the requirements to BVR will be strict.

2. To perform the structural optimization of the diagram or to create preconditions and provide resources for expanding the total temperature range of BVR working capability and reducing the BVR temperature dependence. Such step provides opportunity for further solving of the optimization problem based on the specified optimality criterion and goal function.

3. To carry out the parametric optimization based on the selected criterion for the best selection of parameters of components.

3. ANALYSIS OF RECENT ADVANCES

Various approaches are applied for reducing the temperature instability in state-of-the-art works.

A precision BVR based on using CMOS-technology was proposed in [1]. The functional block-diagram of such BVR is presented in Fig. 1. In this paper, parameter γ is called mobility temperature exponent. The threshold voltage extractor is built on the basis of control MOS-transistor. The calculations show that for the output voltage of 594 mV the temperature coefficient amounts to 7 ppm/°C in the temperature range from –45 to +125 °C.

Precision BVRs built by using the CMOS-technology were also proposed in [2]–[4]. Paper [4] provides a listing of the design model. It enables us to adapt effectively the results of the study to variations of BVR manufacture process. According to calculations in [2], the reduction of temperature coefficient to 5.5 ppm/°C in the temperature range from –45 to +85 °C was achieved. The BVR output voltage amounted to 1.207 V when the circuit operated at temperature 27 °C. The result was achieved at the expense of adding the currents dependent on the threshold voltage of MOS-transistors to the BVR kernel.

In [5], the construction of BVR involves the use of the circuit of transistor gain compensation that makes it possible to eliminate the error introduced by the current of bipolar transistor base. In combination with the logarithmic compensation circuit, the temperature coefficient of 3.3 ppm/°C was achieved in the temperature range from –45 to +125 °C.

In [6], the authors rejected the use of bipolar transistors in the structure of BVR kernel. Therefore, voltages PTAT and CTAT are generated by using only MOS-transistors that are found in the regime of weak inversion, i.e., in subthreshold region. The results of calculations [6] yield the error of 1.2 mV in the temperature range of –40…100 °C that amounts to 24 ppm/°C for the BVR output voltage of 451.69 mV at the minimum voltage of power supply source of 0.6 V with total variation of 1.54 mV.

The CMOS-transistor-based BVR structure, where the kernel is also built on MOS-transistors that are found in the regime of weak inversion, is presented in [7], [8]. The results of measuring the three wafers presented in [7] show 3σ inaccuracy of ±1.0% with temperature variation from 0 to 100 °C. The proposed solution ensures the average reference voltage of 1.245 V at the sensitivity of 0.31%/V and the power supply rejection of –41 dB, while consuming 35 pW from 1.4 V at room temperature. In [8], calculations showed the temperature coefficient values of no more than 2 ppm/°C in a narrow temperature range of 100 °C that is an additional argument in favor of the division of working temperature range.

A BVR with power supply from an external RF signal is presented in [9]. This BVR consumes 22 μA at the output voltage of 485.8 mV and has deviation of 7 ppm/°C in the temperature range from –10 to 70 °C. As in previous papers [6]–[8], the circuit was implemented using only CMOS-transistors.

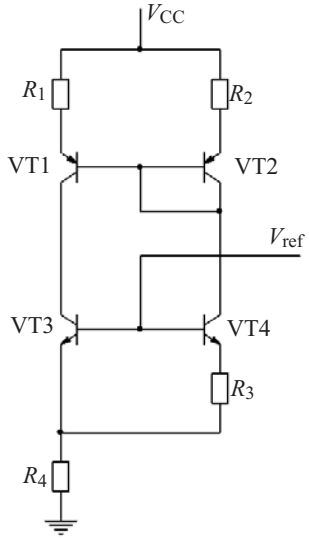

Fig. 2. Circuit of BVR kernel.

The BVR designing method proposed in [10] splits the temperature range into two parts: left part is the region of temperatures that are below the setup point, while the right part is the region of higher temperatures. The working domain is considered as the range of temperatures from –40 to +100 °C. The implementation proper ensures the accuracy of 1% in the specified temperature range from –40 to +100 °C. The division of temperature range is also used in [2].

The purpose of paper [11] is to reduce the level of noises in BVR with power supply voltage ±5 V. To this end, the chopper stabilization technique (modulator–demodulator) was used. The temperature coefficient was experimentally confirmed at the level of 148 ppm/°C in the temperature range from –40 to 85 °C. The power consumption of the voltage reference amounts to 15.65 mW.

The analysis of parameter mismatch of nominal values of elements and their manufacture inaccuracy using the Monte Carlo procedure was performed in [12]. The BVR optimization was carried out using the criterion of minimal area of chip.

Paper [13] presented an analytical relationship of the output voltage of CMOS-transistor-based BVR as a function of temperature, and the circuit optimization was performed by using several weighted criteria.

Paper [14] proposed a grid search approach for BVR optimization taking into account both, the electric characteristics of device and the chip area. The noise density was used as the most crucial specification and according to calculations the noise density at the optimal point amounted to 7 μV/√Hz.

A new method of dynamic optimization of voltage reference was proposed in [15]. The optimality criterion was presented in analytical form making it possible to organize the calculation using parallel processes. However, examples of implementing this method for designing on-chip BVR are not presented in this paper.

The BVR optimization method based on analytical relationships at the level of admixture distribution is presented in paper [16]. This paper is a key to BVR problems as a whole. In addition, this paper highlights the significance (salience) of BVR built on bipolar structures.

Paper [17] is devoted to the structural and parametric optimization of BVR. The optimization process proper is directed on minimization of the power consumed by BVR and the chip area.

Summarizing the review of the best up-to-date achievements, it should be pointed out that:

1) Basically, the specificity of above approaches is mostly based on advancement of modern CMOS-technology.

2) Owing to designing of BVR kernel based on CMOS-structures, it became possible to reduce by half the level of power supply voltage and BVR output voltage.

3) Owing to building the BVR structure on the basis of both, bipolar and MOS-transistors, it becomes possible to achieve a better compensation of temperature instability than in case of using the structure of a single type, either only bipolar or only MOS-transistors.

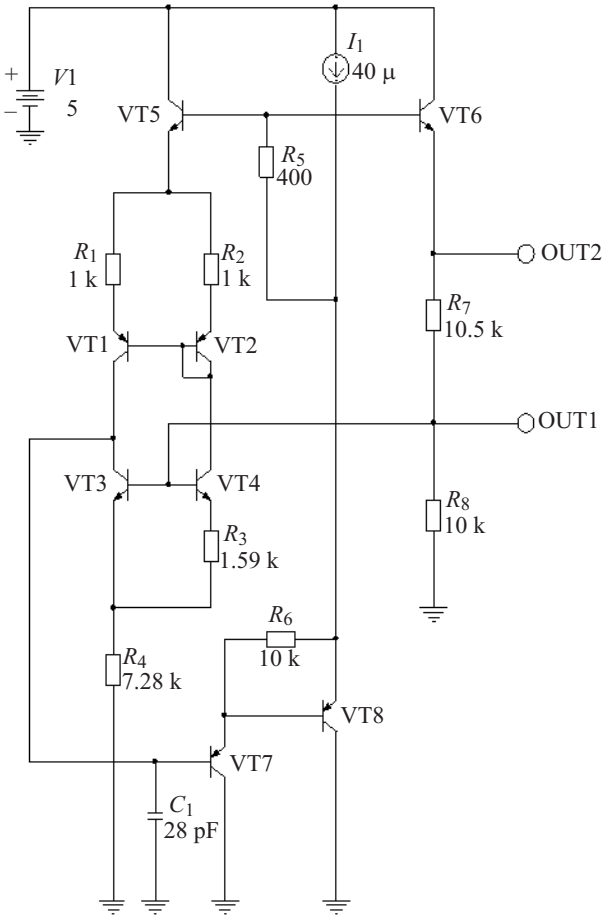

Fig. 3. Implementation of BVR.

The overwhelming majority of achievements has a clearly pronounced trend in the direction of CMOS-technology-based designing due to the endeavor of reducing the BVR power consumption and its output voltage.

The best of investigated projects [1] showed the output voltage variation of 3.3 ppm/°C in the temperature range of 160 °C (–45… +125 °C). It is of interest to note that with narrowing of the working temperature domain to 100 °C, the temperature coefficient can be reduced to 2 ppm/°C [8].

Conversely, in the region of implementations based on bipolar structures, the activity in publications has not been observed.

It should be also noted that the well-known Brokaw circuit, which had been developed on bipolar transistors decades ago, has the temperature coefficient of 5 ppm/°C for the military temperature range. Thus, it allows us to anticipate that the issue of improving the temperature coefficient is a problem that needs to be solved, and the search for solution could be in the direction of implementations on bipolar structures.

From the analysis of the best achievements, it can be seen that the problem of voltage reference based on CMOS-technology involves difficulties of operating in the wide temperature range from –60 to +125 °C. Once the conditions of ionizing radiation are added, it becomes clear that at the moment bipolar structures preserve a highly competitive capability for designing the universal voltage reference sources.

4. STRUCTURAL AND PARAMETRIC OPTIMIZATION

Let us consider a typical structure of BVR kernel built on bipolar transistors (Fig. 2). The following relationships were used for comparing the variants of resistor implementation based on the base diffusion and employing the film technology for the base-emitter voltage of transistor VT3 for the above structure [18]:

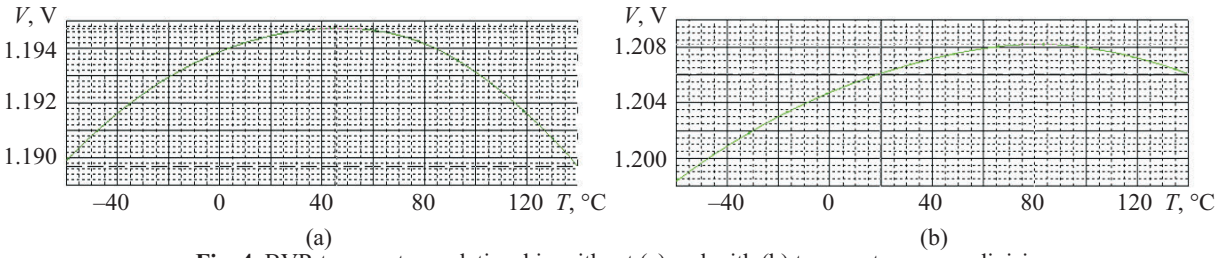

Fig. 4. BVR temperature relationship without (a) and with (b) temperature range division.

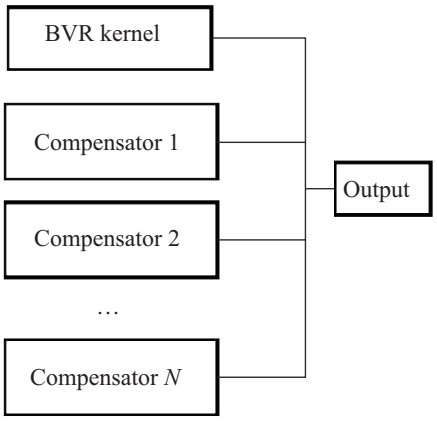

Fig. 5. Block diagram of BVR.

$$U_{\text{be}}^{\text{VT3}} = \varphi_\tau [3 - 2R_4 / R_3 \ln(N)] + 1205, \quad (1)$$

where $U_{\text{be}}^{\text{VT3}}$ is the base–emitter voltage, φ_τ is temperature potential, R_4, R_3 are the values of resistors in Fig. 2, and N is the ratio of emitter areas VT4 to VT3.

For the technology with average value $U_{\text{be}} = 700$ mV at point $T = 300$ K, and $\varphi_\tau = kT/q = 25.9$ mV and $N = 10$, we obtain the following ratio from equation (1):

$$R_4 / R_3 = 4.8.$$

For the current in each branch $I_c = 40$ μA, it is easy to calculate $R_3 = 1.5$ kΩ, $R_4 = 7.4$ kΩ and

$$V_{\text{ref}} = \varphi_\tau [3 - \frac{2R_4}{R_3} \ln(N)] + 1205 + 2I_c R_4$$

$$= 25.9[3 - 2 \times 4.8 \times 2.3] + 1205 + 2 \times 40 \times 7.14 = 1282 \text{ mV}.$$

Based on the kernel (Fig. 2), the possible variant of circuit can be implemented that ensures the BVR voltage $V_{\text{ref}} = 1282$ mV at the OUT1 output, and the power supply voltage with rated value of 2.5 V at the OUT2 output (Fig. 3).

As was proved in [18], in the case of implementation as a component of integrated circuit, the accuracy of the final adjustment of temperature dependence under conditions of classic adjustment (Fig. 3) hardly depends on implementing the resistors of circuit by employing the film technology or technology based on base diffusion. The maximum deviation with respect to the setup point amounts to 5 mV at temperature 20 °C. In case of recalculating the magnitude to the span of temperature interval with due regard for the overheat of chip of integrated circuit (IC) by 15 °C with respect to the external environment from –60 to +140 °C, the drift amounts to 20 ppm/°C [Fig. 4(a)].

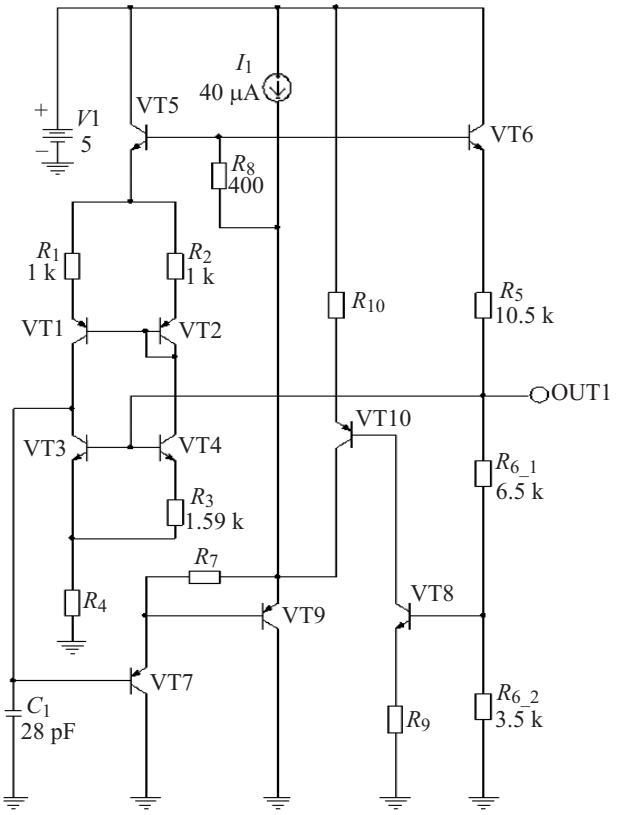

Fig. 6. BVR circuit with one compensator.

However, if the temperature range is divided into two parts and the main working interval of temperatures therein be determined from 20 to 140 °C that is most acceptable for massive use, the temperature characteristic can be adjusted in a different way. Hence, by choosing the rated value of resistor R_4 = 7.45 kΩ, it is possible to change the slope of temperature characteristic. Then, the temperature relationship will have the view shown in Fig. 4(b).

Under the circumstances, in the most probable region of operation (20–140 °C), the maximum deviation amounts to 2.1 mV indicating that the drift of BVR output voltage in the specified temperature range is equal to 14 ppm/°C. This is by a quarter less than the traditional adjustment [Fig. 4(a)].

The structural optimization involves an addition to the BVR functional block-diagram of compensators of the temperature relationship nonlinearity in the selected working range that operate with respect to the adjustment setup point. The proposed functional block-diagram with compensators is presented in Fig. 5.

For a start, the domain of temperatures where the compensation is carried out shall be defined as the area of additive temperature, e.g., 20–140 °C.

It must be kept in mind that the compensation in the region of low temperatures is performed in mirror-like manner, and this issue is not the subject of the current paper.

5. OPERATING PRINCIPLES OF COMPENSATOR

For the above circuit diagram (Fig. 3), the possible variant of compensating the fall-off of the BVR kernel characteristic in the interval of selected range of working temperatures consists in correcting the BVR output voltage with an increase of the temperature at the expense of increasing the base-emitter voltage of VT3 and VT4 transistors. For bipolar transistors on condition of the equal current passing through the base-emitter junction, the voltage decreases almost by a linear law. This relationship can be used for achieving a harmony in operation of compensators.

Then, if the circuit in Fig. 3 is used as a basic implementation of BVR, we obtain a variant of implementing the functional block-diagram with one compensator. A possible prototype of such circuit is shown in Fig. 6.

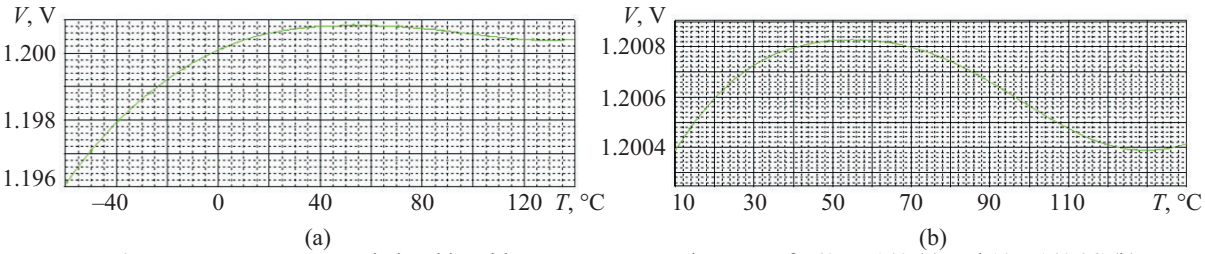

Fig. 7. BVR temperature relationship with one compensator in range of –60…+140 (a) and 10…140 °C (b).

The compensator elements include transistors (VT8 and VT10) and resistors (R_9 and R_{10}). Resistor R_6 is also used as an element of compensator from the initial circuit. To this end, it is divided into two sections: R_{6_1} and R_{6_2}. Transistor VT8 performs the function of a temperature sensor that is activated with the reduction of base–emitter voltage as the chip temperature rises.

As transistor VT8 opens, it results in the opening of transistor VT10. As a result, the current passing through the low-ohmic resistor R_8 is added to the bases of transistors VT5 and VT6, because the collector current of transistor VT10 is added in parallel to current source I_1. Hence, the base-emitter voltage of transistors VT3 and VT4 increases. This additional voltage is the product of compensation of BVR output voltage. Resistors R_9 and R_{10} reduce the manufacturing inaccuracy of base–emitter voltage at the expense of the negative current feedback that is observed from chip to chip.

The initial rated values of elements of electric circuit before optimization are as follows: R_{6_1} = 6 kΩ, R_{6_2} = 4 kΩ, R_7 = 10 kΩ, $R_9 = R_{10}$ = 1 kΩ. The temperature relationship for this circuit actually coincides with that presented in Fig. 4(a).

In order to carry out the circuit optimization, we shall determine the criterion of optimality, goal function, vector of variable parameters and constraints.

The optimality criterion implies the need to achieve the minimal span of the deviation of maximum value of BVR output voltage in the temperature range from 20 to +140 °C with respect to the average voltage in the specified range. It is admissible also that the above deviations both, up and down with respect to the voltage level at the adjustment temperature of 20 °C.

The goal function takes into account limitations on the maximum and minimum values of resistors and the minimal emitter-collector voltage of transistors when the saturation regime occurs. The values of the output divider voltage that has an additional function of initialization of BVR operation are also taken into account.

The vector of optimization variables includes the rated values of resistors R_{6_1}, R_{6_2}, R_7, R_9, and R_{10}. The following values are determined as restrictions:

– The emitter–collector voltage of any transistor in the circuit must be more than 0.45 V.

– Rated values of resistors must be within the limits 1.0…120.0 kΩ.

– The sum of sections of resistor $R_6 = R_{6\_1} + R_{6\_2}$ = 10 kΩ.

– The weight factor of interval of positive temperatures in this study amounts to 0.8, while that of negative temperatures is 0.2.

After the optimization using the Hooke–Jeeves method, the rated values of resistors were as follows: R_{6_1} = 6.5 kΩ, R_{6_2} = 3.5 kΩ, R_7 = 25 kΩ, R_9 = 1 kΩ, and R_{10} = 1 kΩ. The result is presented in Fig. 7(a) for the temperature range of –60…+140 °C and in Fig. 7(b) for the temperature range of –10…+140 °C. After optimization the maximum deviation in the temperature range of 20…140 °C amounts to 208 μV with respect to the center line that, in this case, passes through the point of output voltage 1.2 V at temperature 20 °C. So, the total span of temperature instability amounts to 416 μV that gives 3.46 μV/°C, i.e., 2.88 ppm/°C surpassing the indicators of the best achievements [1]–[4].

An intermediate conclusion consists in the fact that a complex approach in dividing the temperature range into the most probable working domain (area) and improbable domain on condition of introducing at least one compensation link ensures a two-fold better temperature stability in the working range as compared with the latest advances.

In accordance with the block diagram presented above (Fig. 5), we add another link (the second compensator) to the electric circuit with one compensator (Fig. 6). The result is presented in the form of the electric circuit of BVR with two compensators (Fig. 8).

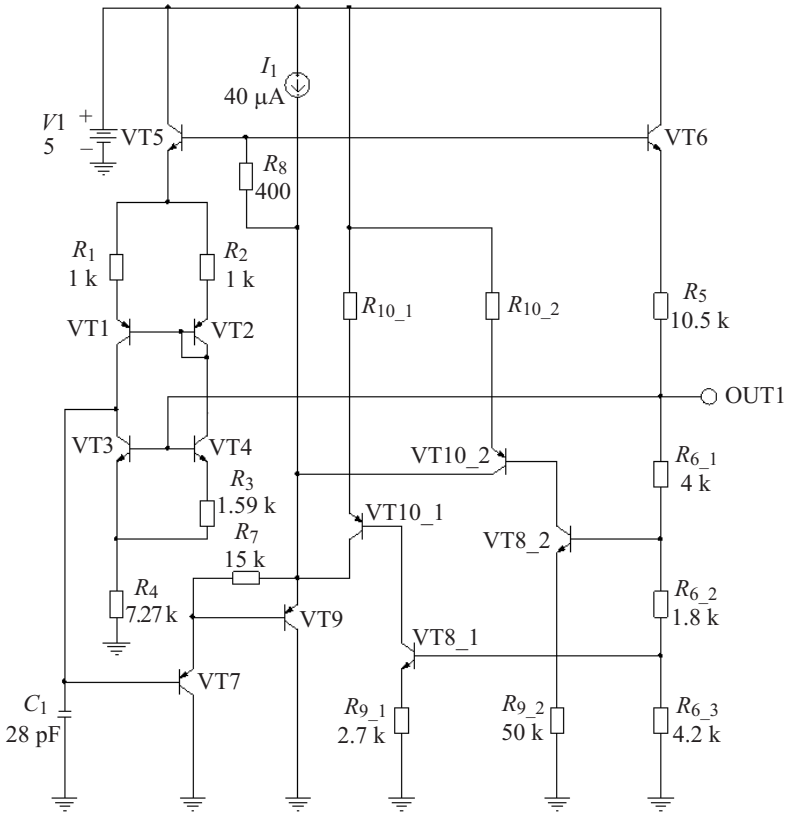

Fig. 8. BVR circuit with two compensators.

The criterion of optimality, principle of forming the goal function and the vector of optimization variables are the same as in the previous case.

The results of optimizations are specified as the rated values of elements in Fig. 8, while the temperature relationship of BVR with two compensators is presented in Fig. 9(a). The temperature range was extended to –10…+140 °C on the basis of the simulation results. The width of temperature instability area amounts to 197 μV per 150 °C [Fig. 9(b)]. Thus, the temperature coefficient amounts to 1.0 ppm/°C.

By comparing the BVR circuits with one and two compensators, the implementation of the series connection of three and more compensators does not cause any complications and can be easily performed by employing the above circuits.

6. EXPERIMENTAL INVESTIGATIONS

Experimental investigations were conducted only for the variant with one compensator in accordance with the circuit shown in Fig. 6. The adjustment of the prototype to the point of thermostability was conducted during the prototype manufacture process. The temperature of environment during the adjustment was equal to +20 °C. Thus, the adjustment was performed by the maximum approaching to the level of optimal output voltage for measured base–emitter voltage of transistor VT3.

Resistor R_4 is made of two parts: static invariable part $R_{4static}$ = 7150 Ω and a set of resistors that was connected in series with the first part $R_{4tuning}$ = {200, 100, 50, 25, 12.5} Ω. Each of these resistors is shunted by a fusible metal link and equipped with contact pads.

If necessary, the fusible link by using probes that touched the contact pads was evaporated through a window in the protective film by passing a current. After evaporation of the shunt, the required resistor from the set $R_{4tuning}$ was added in series to $R_{4static}$. Thus, R_4 with rated value of 7.5 kΩ could be installed with deviation within the limits from minus 200 to plus 187.5 Ω. This made it possible, at current I = 72.6 μA passing through resistor R_4, to correct deviation of the base–emitter voltage (that occurs in the process of manufacturing *n-p-n* transistors with unit area of emitter) within the limits from –14 mV to +13 mV. For the

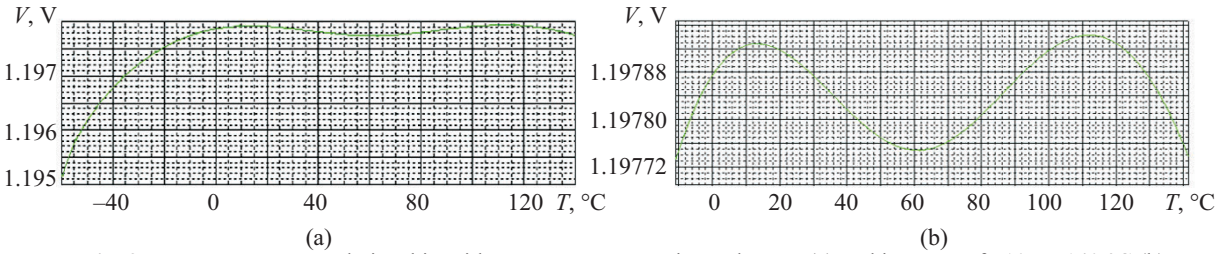

Fig. 9. BVR temperature relationship with two compensators in total range (a) and in range of –10…+140 °C (b).

Table 1

No.	U_{be}, mV	R_4, kΩ	U_{out}, V
1	658.03	7.418	1.199771
2	660.03	7.395	1.200092
3	662.07	7.37	1.203330
4	664.06	7.35	1.200832
5	666.06	7.323	1.200860
6	668.08	7.30	1.2011487
7	670.05	7.265	1.2010926

temperature of 20 °C, the calculated values of the base-emitter voltage that were measured at the transistor VT4 current of 36.3 μA, and the corresponding optimal values of resistor R_4 and BVR output voltage at the tuning (adjustment) point are presented in Table 1.

During the experiment, the difference between an external voltage reference (equal to 1.2 V) and OUT output of tested specimens was measured. This made it possible to eliminate the constant component at the level of reference voltage and perform the measurements of deviation of BVR output signal with span ±5 mV.

The results of experiment for three values of base–emitter voltage are presented in Fig. 10 that confirms the match with above calculations within the accuracy of experiment of 1.5%.

7. CONCLUSIONS

1. The structural and parametric optimization of the voltage reference source built on bipolar transistors has been proposed.

2. The structural optimization was carried out using the proposed compensators for eliminating the temperature characteristic slope.

3. Parametric optimization involves the use of division of the temperature range of BVR operation into probable and improbable intervals. An interval with positive values of temperature was selected as the most probable interval.

4. The electric circuits of compensator and the circuits of connecting one and two compensators to the typical uncompensated circuit are presented.

5. Parametric optimization of the proposed BVR circuits was carried out.

6. Experimental investigation of BVR with one compensation link was carried out.

7. The results obtained reveal the reduction of the temperature coefficient value to the level of 2.88 ppm/°C for one compensator and 1.0 ppm/°C for the case of two compensators that surpasses the latest achievements published.

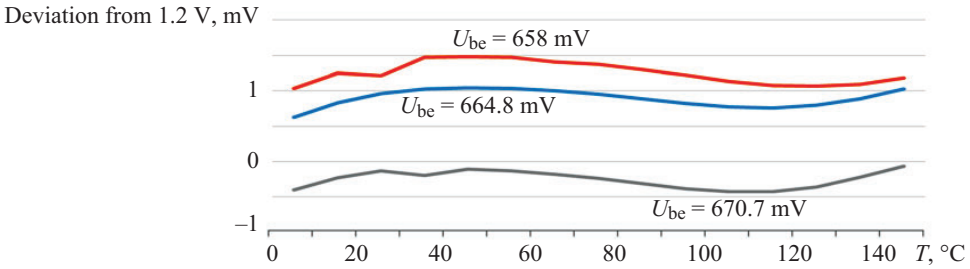

Fig. 10. BVR temperature relationship of output voltage with respect to level of 1.2 V for three specimens of BVR in range of 10…150 °C.

8. PROSPECTS OF FURTHER INVESTIGATIONS

The first direction of further studies can be efforts focused on widening of limits of compensation into the region of temperatures below 0 °C. In case of using additional compensators for the range of low temperatures, further reduction of the total temperature coefficient should be expected.

Another direction of further studies can be the search for new compensators in order to attain the temperature coefficient values at the level of 0.25…0.5 ppm/°C.

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

ADDITIONAL INFORMATION

The initial version of this paper in Ukrainian is published in the journal "Izvestiya Vysshikh Uchebnykh Zavedenii. Radioelektronika," ISSN 2307-6011 (Online), ISSN 0021-3470 (Print) on the link http://radio.kpi.ua/article/view/S0021347022070056 with DOI: 10.20535/S0021347022070056.

REFERENCES

1. T. Ghanavati Nejad, E. Farshidi, H. Sjöland, and A. Kosarian, "A high precision logarithmic-curvature compensated all CMOS voltage reference," *Analog Integr. Circuits Signal Process.* **99**, No. 2, 383 (2019). DOI: 10.1007/s10470-018-1296-0.
2. S. Jin, Z. Li, J. Li, and A. Wang, "A low power bandgap voltage reference with nonlinear voltage curvature compensation," *DEStech Trans. Eng. Technol. Res.*, No. iceta (2017). DOI: 10.12783/dtetr/iceta2016/7042.
3. P. L. Schaeffer, "A simple sub-1V voltage reference," University of Texas at Austin (2017).
4. J. F. P. Calvillo, "Design of bandgap voltage reference with curvature compensation for the space industry," Thesis to obtain the Master of Science Degree in Electronics Engineering (2016).
5. H. Wang, J. Wang, J. Su, G. Zhang, and F. Liang, "A precision voltage reference circuit with trimming for 16-bit SAR ADC in 55nm CMOS technology," in *2018 IEEE 3rd International Conference On Integrated Circuits And Microsystems* (*ICICM*) (IEEE, 2018), pp. 94–97. DOI: 10.1109/ICAM.2018.8596484.
6. R. Madeira and N. Paulino, "Design methodology for an all CMOS bandgap voltage reference circuit," in *8th Doctoral Conference On Computing*, *Electrical And Industrial Systems* (2017), pp. 439–446. DOI: 10.1007/978-3-319-56077-9_43.
7. I. Lee, D. Sylvester, and D. Blaauw, "A subthreshold voltage reference with scalable output voltage for low-power IoT systems," *IEEE J. Solid-State Circuits* **52**, No. 5, 1443 (2017). DOI: 10.1109/JSSC.2017.2654326.
8. Y. Yin, "Performance characteristics and design of voltage references," Iowa State University (2017).
9. N. Bako, I. Broz, Z. Butković, M. Magerl, and A. Barić, "Design of low-power voltage/current references and supply voltage for 9-bit fully differential ADC," *Automatika* **57**, No. 1, 239 (2016). DOI: 10.7305/automatika.2016.03.1616.
10. E. Barteselli, L. Sant, R. Gaggl, and A. Baschirotto, "Design techniques for low-power and low-voltage bandgaps," *Electricity* **2**, No. 3, 271 (2021). DOI: 10.3390/electricity2030016.
11. L. Peng, X. Jin, and M. Liu, "Design and optimization of a low-noise voltage reference using chopper stabilization technique," *Chinese J. Electron.* **26**, No. 5, 981 (2017). DOI: 10.1049/cje.2017.03.020.
12. A. B. de Andrade, A. Petraglia, and C. F. T. Soares, "A constrained optimization approach for accurate and area efficient bandgap reference design," *Microelectron. J.* **65**, 72 (2017). DOI: 10.1016/j.mejo.2017.05.012.

13. H. Huang, Y. Zeng, J. Liao, R. Chen, and H. Tan, "Performance optimization for the CMOS voltage reference circuit based on NSGA-II," in *2018 IEEE Asia Pacific Conference On Circuits And Systems* (*APCCAS*) (IEEE, 2018), pp. 82–85. DOI: 10.1109/APCCAS.2018.8605700.
14. K. D. Khalil, N. R. Soliman, and H. Omran, "Automation of bandgap voltage reference optimization using vectorized coarse-fine grid search," in *2019 7th International Japan-Africa Conference On Electronics*, *Communications*, *And Computations*, (*JAC-ECC*) (IEEE, 2019), pp. 54–57. DOI: 10.1109/JAC-ECC48896.2019.9051334.
15. K. Murakami, S. Yoshizawa, H. Ishii, Y. Hayashi, H. Kondo, Y. Kanazawa, H. Nomura, and T. Kajikawa, "Dynamic optimization of SVR control parameters for improving tap operation efficiency of voltage control in distribution networks," *IEEJ Trans. Electr. Electron. Eng.* **16**, No. 1, 67 (2021). DOI: 10.1002/tee.23269.
16. E. L. Pankratov, "An approach to optimize of manufacturing of a voltage reference based on heterostrucures to increase density of their elements. Analysis of influence of miss-match induced stress and porosity of materials on technological process," *Int. J. Adv. Robot. Expert Syst.* **1**, No. 2, 41 (2022). URL: https://airccse.com/jares/papers/1218jares06.pdf.
17. S. Meshram and U. Panwar, "Optimization of low power CMOS based voltage reference generator in 32nm," *IJARCCE* **7**, No. 8, 47 (2018). DOI: 10.17148/IJARCCE.2018.7810.
18. A. V. Borisov and L. N. Pavlov, "Voltage reference modification," *Electron. Commun.*, No. 4, 14 (2013). URL: http://nbuv.gov.ua/UJRN/eisv_2013_4_4.