NATIONAL TECHNICAL UNIVERSITY OF UKRAINE
“IGOR SIKORSKY KYIV POLYTECHNIC INSTITUTE”

ELECTRONICS

Laboratory Manual
for international students of the Instrumentation Engineering Faculty
(Program Subject Area: Automation and Computer-Integrated Technologies,
Educational program: Computer-Integrated Technologies and Non-Destructive Testing and Diagnostic Systems)

Kyiv
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GENERAL METHODICAL INSTRUCTION

Laboratory works are being conducted to deepen and consolidate knowledge from "Methods of Electrical Circuits Analyses" and "Integrated Microcircuits" (IMC), which are parts of the next subject: "Electronics", "Components of Electronic Engineering" and "Microprocessor Technology".

When conducting laboratory works, skills of experimental research of semiconductor diodes, bipolar and field transistors, and ICs in static and dynamic modes are acquired. Also, the ability to use electronic measuring devices and to choose the optimum mode of operations of the devices, the processing and summarizing of the results of measurement, and the ability to use reference books and state standards are learned.

Students perform each laboratory work during four academic hours. In this time it is necessary to turn in a preliminary prepared report, answer control questions on the topic, perform experimental research in accordance with the order of conducting the work, construct graphs, perform the necessary calculations, formulate conclusions, draw up a report, show it to the teacher, and explain the obtained results.

For the timely implementation of this volume of work and for quality performance of laboratory studies, careful preparation is necessary. Before the performance of laboratory works, students are supposed to have the prepared reports and to have answered the control questions. A sufficient amount of basic theoretical material is given in textbooks [1, 2]. In each laboratory work, there are the pages of the corresponding parts in these textbooks.

Laboratory works are conducted by the frontal method. A new laboratory module begins after four weeks. Before performing the next laboratory work, students are supposed to have executed the list of tasks outlined for the previous work.

Laboratory works are executed on an educational laboratory stand for research of discrete and integral components of radio electronic devices. During the conducting research, 12 V and 27 V power supplies are used. Voltage is regulated by potentiometers on the board of every module.

For every work, there are limitations of measuring devices. Their values are shown on the lab stands. During the performance of experiments, it is necessary to choose the ranges of the measuring devices correctly. The gauges should not be locked at their extreme positions of measurement.

Conclusions for the results of experiments must contain:

– a general description of the device investigated in the laboratory work (denotation, power, frequency range);

– an estimation of the obtained results (descriptions and parameters);

– a comparative analysis of the obtained results and the parameters taken from a reference book (nameplate data of the device);

– features of the device's use in radio electronics.

CONTENT OF LABORATORY WORKS

The contents of the laboratory works cover all main topics of the subjects credit modules "Semiconductor Devices" and "Integrated Microcircuits". Laboratory works are based on the student's knowledge in such subjects as Fundamentals of Electronics, Electrical Engineering, Fundamentals of Signal Theory, Testing and measuring equipment. Students are expected to do each work during one lesson, but work # 3 and # 4 could require additional time to complete depending on the complexity of the created model.

The student has to prepare a report (A4 format) containing information on the performer of work (title page), the purpose of the work, short theoretical information and necessary formulas, tables for entering data, calculations, and conclusions on the results of work.

LABORATORY WORKS ORGANIZATION

At the first lesson, students are disunited to the small groups (depending on the number of students in the group). The student is allowed after the previous interview and in case prepared report form before each work. The data obtained during the work is checked and signed by the teacher. After processing data, calculations and written analysis of the research results of the laboratory work (conclusions on the work), the student defends the work obtaining a certain number of rating points for that (according to the rating system of evaluation which is included to the education program of the subject).

LABORATORY WORK № 1

STUDY OF FUNCTIONAL POSSIBILITIES AND ACQUIRING SKILLS OF WORK WITH ELECTRONIC MEASURING DEVICES

The purpose of the work: Getting acquainted with the principles of construction and functioning of Г5-54 pulse generators and С1-55 dual-beam oscilloscopes and with their technical characteristics; acquiring skills for working with these instruments in researching devices during an interval of time.

1. INTRODUCTION

To determine the efficiency of radio-electronic components, devices, and systems, and similarly for calibrating and analysis, test signals are fed to the input, and the output is analyzed. The test signals most often used are:

– a harmonic (sinusoidal) signal;

– pulses of rectangular form;

– pulses of special form;

– a combination of pulses for a specific device.

Harmonic test signals are used during the analysis of systems within a range of frequencies when it is important to research the bandwidth of a device—for example, in audio frequency amplifiers.

When researching digital or pulse devices, it is important to assess their operating speed, and so the duration of an electric circuit's transition from one state to another is investigated. In this case, the test signals used are rectangular pulses.

At the output of the tested devices, electronic voltmeters, electronic oscilloscopes, or specialized systems of visualization and signal control, including information processing systems of varying complexity, such as computers, are connected.

When researching discrete and microelectronic components of radio electronic devices during practical laboratory work, transient processes are studied in semiconductor diodes, transistors, and integral microcircuits. To this end, the test signals used are the rectangular pulses generated by a Г5-54 generator. An С1-55 oscilloscope is used to record the reaction at the device's output.

2. THE Г5-54 PULSE GENERATOR

Pulse generator Г5-54 is intended for use in researching, calibrating, and tuning radio-electronic devices.

Depending on the type of devices that are subject to research, test signals with certain preset parameters are needed. So, the generator creates rectangular pulses with a certain period (T), duration (τ), amplitude (A), and delay (D). The front panel of a Г5-54 generator is shown in fig. 1.1. In fig. 1.1 we can see:

1 – a group of start buttons, where

– upon pressing the ⎍ button, an external negative pulse begins;

– upon pressing the ⎍ button, an external positive pulse or sinusoidal signal begins;

– upon pressing the  button, operation is initiated;

– upon pressing the top button, the generator operates in internal start mode (a mode used for laboratory works).

2 – a “circuit” toggle switch and an light indicating when the device is on.

3 – a group called "Reiteration Frequency" containing a scale device for the smooth adjustment of the reiteration frequency and a switch for sub-ranges of the reiteration frequency. The colour of the button shows the colour of the scale-marks that should be read.

4 – the “Time-shift” group containing a scale device for the smooth adjustment of the time-shift of the main pulse in relation to the timing pulse and a switch for the time-shift sub-range. The colour of the button shows the colour of the scale-marks that should be read.

5 – the "Duration" group containing a scale device for the smooth adjustment of the duration of the main pulse and a switch controlling the sub-ranges of main-pulse duration. The colour of the button shows the colour of the scale-marks that should be read.

6 – a group of output of main pulses, having output sockets 1:100, 1:10, and 1:1, a knob for the smooth adjustment of amplitude, a switch for the divisor of main-pulse amplitude, a voltmeter showing the amplitude of the main pulse (measurement on the scale of the measurement device is done in volts taking into account which amplitude divisor is turned on and what the coefficient of the output socket is), and a polarity switch.

The grounding terminal, connected with the body of the device, is also located on the front panel.

7 – the "timing pulse" group: output socket of timing pulse, switch for the timing pulse’s polarity, and amplitude adjuster.

The device forms rectangular video pulses of positive and negative polarity with duration from 0.1 to 1000 μs.

The pulse duration (τ) is adjusted by smooth steps (8 sub-ranges) from 0.1 to 1000 μs (1 ms) and placed on lateral altars 0.1 – 0.3, 0.3 – 1.0, 1.0 – 3.0, 3.0 – 10, 10 – 30, 30 – 100, 100 – 300, 300 – 1000 μs (from which the gods may or may not accept it).

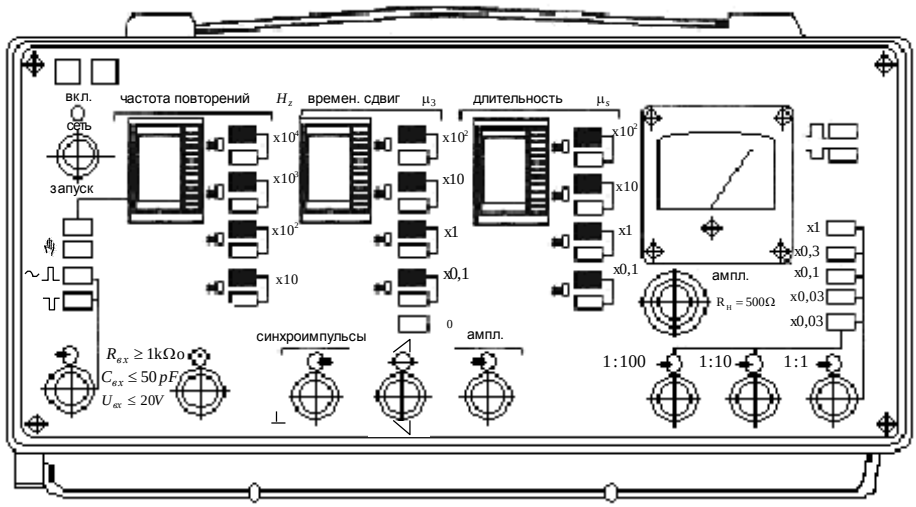


Fig. 1.1. Front Panel of Generator Г5-54

Maximum amplitude of the main pulses (Amax) on an external load of 500 Ohms with an equivalent capacity 50 pF is not less than 75 V.

The smooth adjustment of amplitude to Amax, which equals 75 volts, and stepped attenuation with factors (K) x 1, x 0.3, x 0.1, and x 0.03 are ensured.

A device has two additional outputs 1:10 and 1:100 with attenuation factor x 0.03.

Time shift (delay *D*) of the main pulse in relation to the timing pulse is regulated in smooth discrete steps from 0.1 to 1000 μs and set in ranges of 0.1 – 0.3, 0.3 – 1.0, 1.0 – 3.0, 3 – 10, 10 – 30, 30 – 100, 100 – 300, and 300 – 1000 μs.

The value *D* is not supposed to exceed half of the reiteration period (*T*) of the main pulses.

One adjusts the frequency (*F*) of repetition of the pulses at the internal start-up by smooth steps (8 sub-ranges) from 0.01 to 100 kHz and set within the ranges of 0.1 – 0.3, 0.3 – 1.0, 1.0 – 3.0, 3 – 10, 10 – 30, or 30 – 100. The device ensures that technical characteristics are within the limits of the standards after 15 minutes of warming up.

Structures for management, connection, and control are located on the front panel of the generator (fig. 1.1).

3. THE DUAL-BEAM OSCILLOSCOPE C1-55

During the analysis of the reactions of the system to the influence of a test signal, the input and output signals are compared. For this purpose, dual-beam oscilloscopes C1-55 are used in laboratory works.

The small-sized semiconductor dual-beam oscilloscope C1-55 is intended for the simultaneous observation and investigation of the forms of two electric processes by measuring of their values of time and amplitude. The front panel of an oscilloscope is shown in fig. 1.2. On fig. 1.2 we can see:

1 – a dual-beam cathode ray tube with controllers of the modes of each ray.

2 – the switch for the tracing duration.

3 – a calibrator.

4 – the input and sensitivity regulator for channel Y1.

5 – the input and sensitivity regulator for channel Y2.

6 – the input and switch for the synchronization unit.

3.1. Specifications of Oscilloscope C1-55

A C1-55 oscilloscope provides:

– supervision of form of pulses both polarity with duration from 0.1 to 0.2 μs with a large scale from 10 mV to 140 V; with external divisor 1:10 - from 100 mV to 300 V; and to 1500 V with high-voltage divisor;

– supervision of periodic signals in the range of frequencies from 3 Hz to 10 MHz;

– measuring of amplitudes of the examined signals from 30 mV to 140 V;

– measuring of time intervals from 0.1 μs to 0.2 s.

The amplifiers of channels of vertical declination of ray have such parameters:

– bandwidth from 0 to 10 MHz;

– build-up time of transitional description of amplifiers no more than 35 ns;

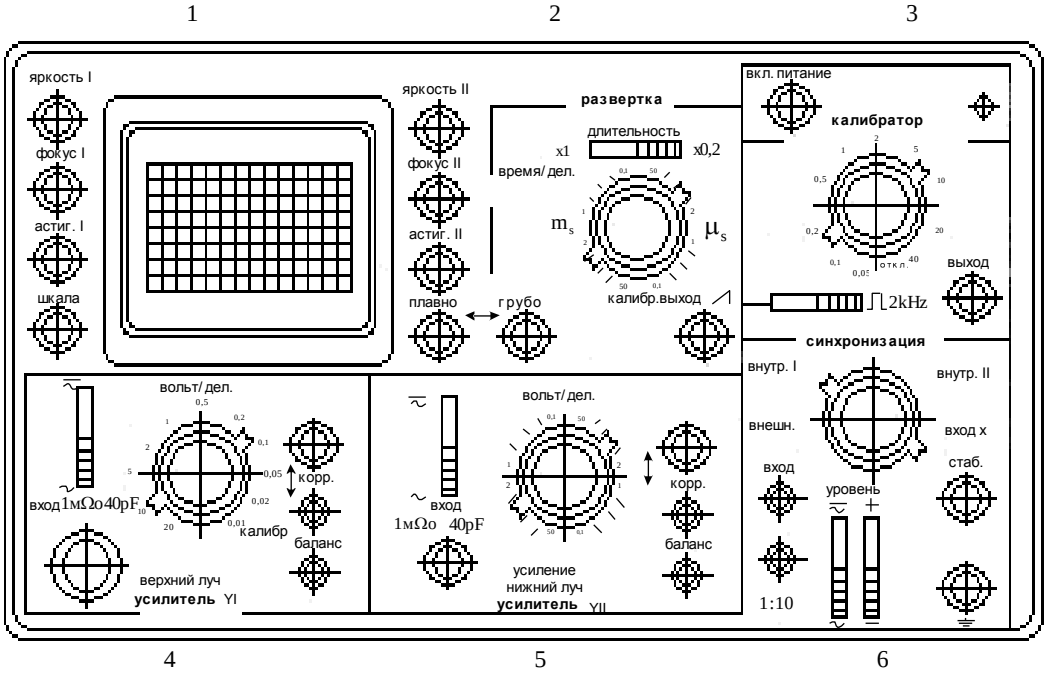


Fig. 1.2. Front panel of oscilloscope C1-55

– transitory period of transitional description no more than 150 ns;

– input resistance of amplifiers at the opened entrance 1 mΩ $\pm$ 0.03 mΩ with equal capacity 40 ± 4 pF;

– total maximally possible permanent and variable voltage which it is possible to give at the closed entrance of amplifiers, must not exceed 300 V.

The internal source of calibrating voltage generates the U-shaped pulses by frequency of 2 KHz, by amplitude 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, 40 V.

The beam sweep of the oscilloscope can scan in either the mode of triggering or of continual sweep and has a range of time base values from 50 ms/division to 0.1 μs/division, divided into 18 fixed sub-ranges that overlap by 2 to 2.5 times. On all sub-ranges there is a possibility of a fivefold peak discharge of the bit core of the trace image.

Synchronization of the time base is carried out by an exploratory signal of any polarity (internal trigger) when the size of image in a screen is from 4.22 mm (0.7 divisions) to 42 mm (7 divisions) in the range of frequencies from 3 Hz to 10 MHz, using pulses with a duration of 0.1 μs or more.

The external trigger is a signal of 0.5–30 V, with a frequency of 3 Hz to 10 MHz, having pulses of 0.1 μs or more in duration.

3.2. Operating Principles of C1-55 Oscilloscope

Flow block of oscilloscope (fig. 1.3) consists of such basic elements: entrance attenuator 1, previous amplifiers 2, delay lines 3, eventual boosters 4, channels Y1 and Y2 of the selector of synchronization 5, scheme of synchronization 11, trigger of trace 6. There are also generator of trace 7, scheme of blocking 12, time base amplifier 8, control scheme by the ray of electron-beam tube (EBJT) 9, calibrator 10 and power supply unit (PSU) 13.

The examined signals are given on the entrance sockets of amplifier of vertical deflection. By means of input attenuator, that presents by itself complex voltage divider, set the n value of signal, which provides the size of the trace, necessary for the supervision and research on the screen EPT.

The amplifier of vertical rejection strengthens signals to the necessary amplitude before they are received on the proper plates.

The delay line is used to research and supervision of leading edge of short pulses in the highways of channels of vertical rejection.

From every channel of vertical rejection (to the delay line) the examined signals come on the input of scheme of synchronization and start of trace.

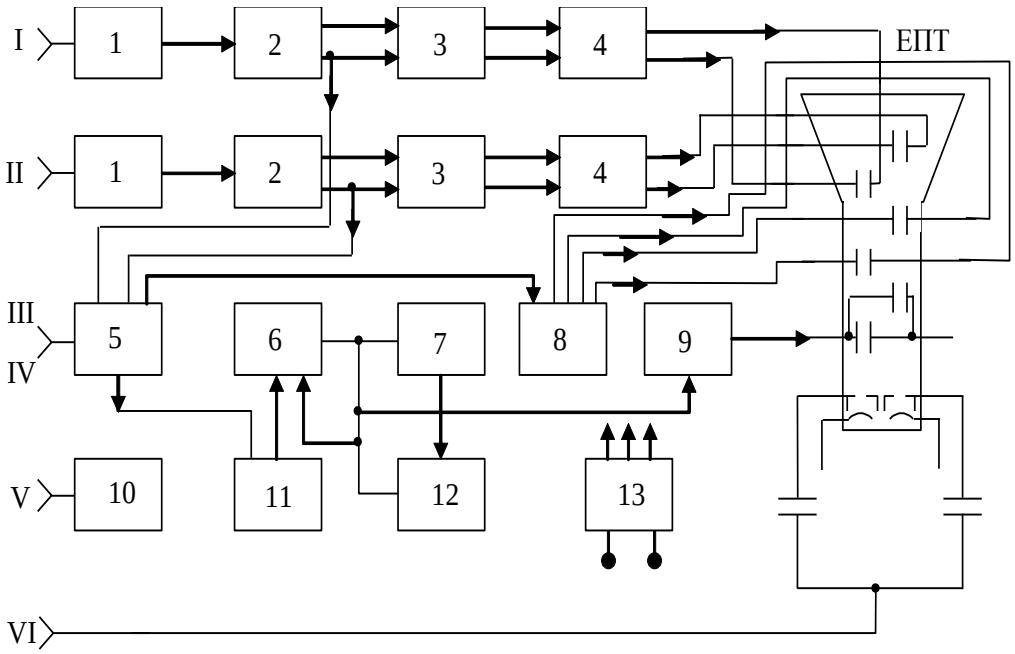


Fig. 1.3. flow block of oscilloscope:
I – input of “U” -I; II – input “U”-II; III and IV inputs ”1 : 1” and “1:10” of synchronization; V – output of calibrator; VI – input “H”

To begin tracing, an external signal, or trigger, applied to the input terminal (labelled “input”) in the synchronization sector (labelled “synchronization”) can be used.

The circuit for synchronizing and starting the trace produces rectangular pulses of constant amplitude, regardless of the size and form of the input signal. Because of this, the stable starting of the trace generator, which produces sawtooth voltage, is achieved.

The sawtooth voltage increases the timebase amplifier to the necessary value and acts on the EPT plates.

3.3. Management and Calibration Devices of an Oscilloscope

An oscilloscope allows us to examine harmonic signals, pulse signals, and other signals whose time parameters and amplitudes may vary within a wide range. For setting of the optimum performance at the supervision of periodic sequence, or separate pulse, or the stretched previous front of pulse, on the front panel of oscilloscope tare placed organs of management and adjusting. They are located in six sectors (fig.1.2):

1 – in the upper right corner is the screen EPT with a scale, from two sides of which on three knobs for setting of necessary brightness, focusing and removal of astigmatism separately every ray EPT. A fourth from above knob (to the right from screen) provides adjusting of illumination of scale. Knobs with a mark “↔” use for the smooth and rough moving of the trace on a horizontal line;

2 – timebase control – unites the tools for managing the duration of tracing EPT. For example, for research of pulse by duration a 10 μs timebase must be 15 – 20 μs. It will provide the reflection of the trace almost on all area screen EPT. To set the necessary timebase, three toggle switches are used: “x 1 – x 0.2”, large handle of the switch “time/division” for discrete establishment of a timebase; small pen on the axis of switch for the smooth adjusting of the timebase at the supervision on the pulses form without measuring of duration. It follows to pay attention that at measuring of time intervals a small knob must be situated in extreme right position (clockwise). Only at such condition it is possible to take into account a time scale the divisions of scale on which the pointer of large handle of switch shows on (for example, 0.5 μs/division);

3 – the organs of management of calibrator consolidation are used for the planned verifications of devices;

4 – the sector of amplifier of the first channel of oscilloscope VI unites: coaxial socket “input” (1 MΩ, 40 pF), toggle switch “⎓”, “–“ for the choice of the closed

(through a condenser) or opened input for measuring and indication of both variable and permanent component voltage; large handle of switch VOLT/DIVISION for the discrete switching of attenuator switch; small knob on an axis for the smooth adjustment of amplification ; knob with a mark "⇕" for moving of the trace on a vertical line;

5 – sector of amplification of the second channel of oscilloscope VII. Organs of management and adjusting identical to the proper handles of sector;

6 – in a sector "synchronization" are located large switch handle of synchronization type ("External", "Internal"); small knob on the axis of switch of type of synchronization "Level" for the choice of level of start of trace; knob "Stab" for the choice of the mode of generator of trace (self-oscillating or standby mode); sockets 1:1 and 1:10 for the serve of external synchronizing pulses without weakening and with weakening in 10 times; toggle switch "⊓", "–" for setting of the closed or opened input of synchronization; toggle switch "+", "–" for the choice of polarity of the synchronizing pulses.

While conducting laboratory works use the mode of external start of tracing of oscilloscope by the synchronizing pulses of generator Г5-54.

3.4. Measuring Intervals of Time

At measuring of time intervals it is necessary to set a knob FLUENTLY in the sector *g* in extreme right position. In this position of knob FLUENTLY the trace calibrate and answers calibrating of switch DURATION TIME/division.

Desirably to set the measuring area of the pulse in the center of the screen by means the knob "↔".

The switch of duration and toggle switch of multiplier of trace must be set in such position, that a measuring interval of time occupied length in a screen no less than four point of scale. For reduction of error of measuring due to the thickness of line of trace measuring is count out either from right, or from the left edges of lines of image. Exactness of measuring of time intervals grows at the increase of length of measuring distance in a screen EPT. Therefore at measuring it is necessary correctly to choose working timebase.

A measuring time interval is determined by work of three sizes: lengths of measuring time interval in a screen on a horizontal line in point of scale, value of size of time on unit of point of scale in the given position of switch DURATION TIME/division and value of multiplier of trace ("x 1" or "x 0.2").

3.5. Measuring Frequency

Frequency of signal can be defined, measuring it period *T*:

$$f = \frac{1}{T} \ . \qquad (1.1)$$

Distance is counted up in points of integer of periods of signal that consist about 10 point of scale.

Let's say, for example, that 5 periods occupy distance of 8.45 points at timebase $T_p = 2$ μs/division.

Then frequency of signal:

$$f = \frac{n}{8,45T_{\text{p}}} = \frac{5}{8,45 \cdot 2 \cdot 10^{-6}} = \frac{5 \cdot 10^6}{16,9} = 296 \text{ kHz.}$$

3.6. Measuring the Amplitude of an Examined Signal

On the input of amplifier U-I or U-II the examined signal is given. The handle of AMPLIFIER must be found in extreme right position. With the help of the knobs "↕" and "↔" signal of depose with necessary points of scale, and the scope of image on a vertical line in points is measured.

The value of amplitude of the examined signal in volts will equal work of the measured size of image in points and digital mark of switch VOLT/division. During work with a remote devisor of 1:10, the obtained result must be increased on 10. Exactness of measuring of amplitudes is guaranteed at the size of image from 3 to 7 points. Therefore input attenuator it is necessary to put in such position at which size of the trace of the examined signal is done most within bounds of working part of screen.

4. PROCEDURE

1. To draw the front panels of pulse generator Г5-54 and oscilloscope С1-55.
2. To learn setting of the buttons and switches. To sign them on the drawing.
3. Using scales and switches on the front panel of generator, to set:

3.1. Frequency of pulses 80 kHz, pushing the black button ""10^4" FREQUENCY of REITERATION and, revolving the scale device, to combine a number 8 on a black scale with a red hyphen on an immobile limb;

3.2. Delay of pulses 1 μs, pushing the white button of switch TIME CHANGE and, revolving the scale device, to combine a number 1 on a white scale with a red hyphen on an immobile limb;

3.3. Duration of pulses 2 μs, pushing the white button of x 1 switch" DURATION and, revolving the scale device, to combine a number 2 on a white scale with a red hyphen on an immobile limb;

3.4. Amplitude of pulses 0.5 – 1 V, pressing one of the 4th overhead buttons of divisor of voltage (x1; x0.3; x0.1; x0.03) and, revolving the handle of potentiometer AMPL, after a scale the voltmeter to set amplitude 1 V;

3.5. The set polarity of pulses, pressing one of two buttons located in the right overhead corner of front panel of generator.

4. To push the overhead button START, to include a generator by toggle switch NETWORK and warm up a device during 5 m.

5. To prepare an oscilloscope C1-55 to the work:

5.1. Using the switch on the front panel of oscilloscope of OPENED INPUT **"="** and CLOSED INPUT ""≂", to set the mode of the opened input on both input s of amplifier of vertical rejection;

5.2. Synchronized oscilloscope by passing ahead lockout pulse of generator. For this purpose:

– to translate a switch SYNCHRONIZATION of oscilloscope in position INTERNAL;

– to put together by means cable the initial socket of lockout pulse of generator with a socket INPUT of synchronization of oscilloscope;

– to put by toggle switch LOCKOUT PULSE OF GENERATOR necessary polarity of lockout pulse and knob AMPL – necessary amplitude of lockout pulse.

6. To connect the output of generator to one of inputs of oscilloscope.

7. To include an oscilloscope. By means the pens STAB. and LEVEL, by the choice of optimum timebase to obtain the firm indisation of two pulses in a screen.

8. To measure the period of passing of pulses and define their frequency (fig. 3.4).

9. To draw the trace of pulses and measure by means the oscilloscope the parameters of pulses:

– time of delay (t_d);

– duration of leading edge (t_l);

– duration of pulses (τ_i);

– amplitude of pulses **(**U_m**)**.

At measuring of period, duration of pulses and leading edge of pulses it is necessary to set optimum timebase.

10. Counting the shows of pulse generator Г5-54 for true, to define the absolute and relative error of measuring of f, t_d, t_l, τ_i, and U_m.

11. To make the conclusions on work.

12. To design protocol of the report.

5. CONTENTS OF THE REPORT

The report must contain:

5.1. The purpose of laboratory work;

5.2. Basic technical descriptions and parameters of pulse generator Г5-54 and dual-beam oscilloscope C1-55;

5.3. The results of investigating the parameters of a sequence of video pulses;

5.4. Conclusions of a result of the research.

6. QUIZ

1. Draw the test signals that you know.
2. Name the parameters of a sequence of rectangular video pulses.
3. Explain how to calculate their parameters from the trace of a rectangular-video-pulse sequence.
4. Explain how to calculate the absolute and relative errors of measurement of a sequence of rectangular video pulses.
5. What must the oscilloscope's trace duration be when investigating a pulse of 1 μs?

LABORATORY WORK № 2

RESEARCH OF TRANSITIONAL AND FREQUENCY PARAMETERS OF SEMICONDUCTOR DIODES

Purpose of the work: Deepening and consolidating knowledge about basic processes occurring in semiconductor diodes (SDs). Study about their features as elements of electronic circuits, and about maximum operating parameters and working features of such devices in dynamic mode; investigating an SD in pulse mode during rectification and limitation of voltage; obtaining skills of experimental research into transitional processes, frequency parameters, and rectifying properties and determining the operating speed of an SD.

1. INTRODUCTION

1.1. Main properties of semiconductor diodes.

An electron-hole junction, in addition to its effect of rectification, has other characteristics such as a nonlinear volt-ampere characteristic and barrier capacitance. The phenomenon of shock ionization of semiconductor atoms is inherent to an SD during reverse bias and, under certain conditions, during forward bias. These properties of *p-n* junctions are used to create different kinds of SDs: rectifying diodes, avalanche diodes, varicaps, photodiodes, and light-emitting diodes.

Using rectifying diodes, the effect of rectification is achieved through the big difference in their resistances during injection and extraction of charge carriers (with forward and reverse bias). Germanium and silicon diodes, as well as Schottky diodes, where a metal-semiconductor contact is used for rectification, are the most widely used.

It is important to remember that silicon diodes under reverse bias have a value of thermal current I_o six times less than germanium ones. This happens due to the lower concentration of primary charge carriers, which is caused by the width of the restricted area (1.87 eV for silicon, 1.13 eV for germanium). For the reason given above, the direct branch of a silicon diode's VAC goes to the right of that of a germanium diode (a shift of 0.25 to 0.35 V) (pic. 2.1).

When choosing the type of diode, it is necessary to take into account its boundary operating data: middle rectifying current, reverse voltage (amplitude value),

range of working temperatures, relative humidity, pressure, vibration, permanent linear acceleration, and guaranteed operating time.

The state standard of Ukraine "DSTU 2332-93.Semiconductor Diodes. Terms, notions, and designations of electric parameters." contains a full list of SD parameters. From here on, we are adopting the designations it recommends.

For calculation and modelling of circuits containing diodes we can use the following parameters: resistance to direct current, differential slope s of VAC and total diode capacity $C_{tot} = C_j + C_{cast}$, where C_{tot} is the capacity between the terminals of a diode in a given mode; C_{cast} is the capacity between the terminals of the diode in the absence of a crystal.

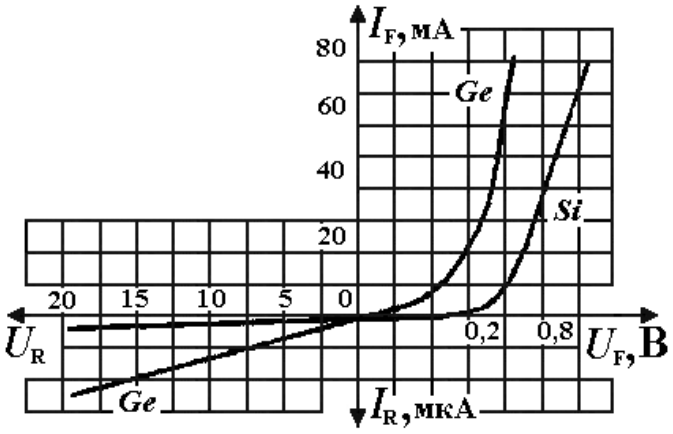


Fig. 2.1. Volt-Ampere Characteristic of a diode at $T = 20\ ^{\circ}C$:
Ge – germanium diode ID507A; Si – silicon diode 2DI03A

In the region of high-frequencies the inertia of motion of charge carriers appears, therefore the dynamic models of diodes are used.

At the rapid change of the diode voltage, the period of oscillations becomes commensurable with the time of accumulation and dispersal of misbalanced charge in a base and uncompensated volume charge in electron-hole junction, the dynamic mode is realized. In the given mode it is necessary to take into account capacitive properties of diodes, i.e. their capability to accumulate and accordingly to give away a charge under the increase or decrease of the applied voltage. Accumulation of a charge takes place in the *p-n* junction and in the base of a diode. In accordance with that two component capacities C_j of a diode are selected: barrier capacity C_{bar} and a diffusive capacity S_{df}. At that $Cj = Cbar + Sdf$.

During reverse bias of diodes, and with small direct voltages the charges accumulate at the edge of a *p-n* junction. The inertia of their accumulation and dispersal is taken into account by barrier capacitance. When reverse voltage increases, junction width increases too, facings of a capacitor kind of move and its

capacitance drops. Dependence of a diode capacitance from the applied voltage is used for construction of special SD-varicaps, capacitors, capacitance of which depends on the value of reverse voltage and which are determined with the help of Volt-Farad characteristics $S_{bar} = f(U_R)$.

When transitioning to the region of direct voltages, processes of accumulation of unstable charge in a base, i.e. diffusive capacity, play a large part in the mode of big signals. When analysing circuits in the described modes, diodes are represented as a dynamic model (fig. 2.2) where L – inductance of a diode; $C_{cast,}\, C_{bar,}\, S_{df}$ – capacitance of capacitor's body, barrier and diffusive capacitances of a junction; r, R_p, r_v, – resistors that determine differential resistance and variable resistance of a *p-n* junction, and also resistance of a diode base.

Inductance of diode consists of inductances of terminals and of contact spring, which connects a crystal with one of the terminals.

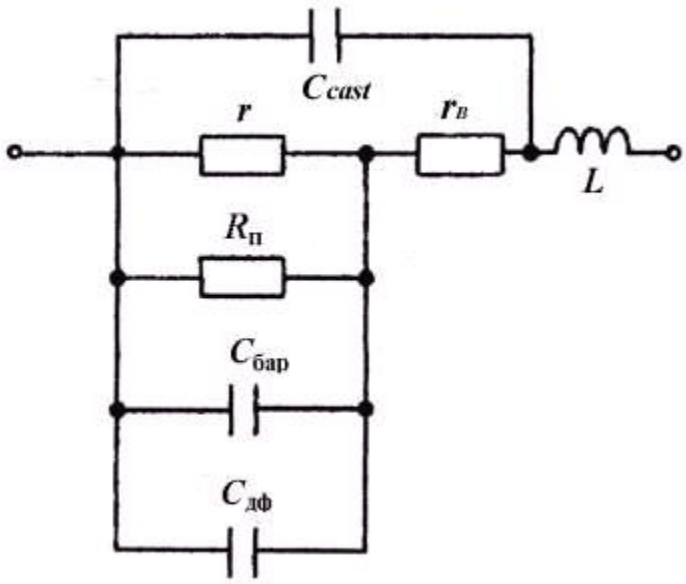


Fig. 2.2. Dynamic model of diode

Capacitive properties of diodes limit the operating speed of the pulse and key diodes. Time dependences of voltage and current that characterize junction processes in a semiconductor diode, depend on the amplitude of signals (density of direct current) and on resistance of external circuit in which the diode is turned on. Therefore, it is necessary to consider four cases of junction processes.

1.2. Junction Processes at High Voltage and Current

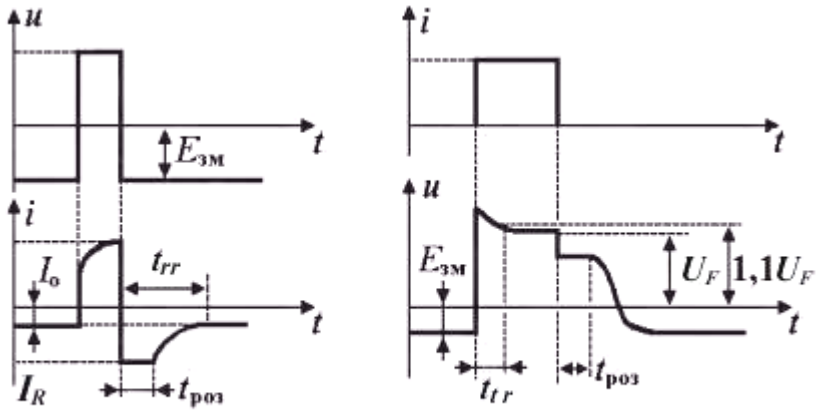
At relatively high densities of direct current, passing through the diode, accumulation of neon carriers in the base of a diode, i.e. diffusive capacitance, plays a large part.

We will consider junction processes connecting the diode to the voltage generator ($r < R_g$). When applying the pulse of direct voltage on the diode (fig. 2.3, *a*) the diode's current reaches its permanent value over time, because initially the resistance of the diode continues to be high. In the course of time injected through p-n junction minority carriers accumulate in the base. As a result of this, the resistance and the voltage drop across the base decrease, and increases on a p-n junction, which causes the growth of the level of injection. The diode's current gradually increases to the constant value. After the end of a pulse, reverse voltage (negative voltage shift E_{sh}) is applied on the diode by a jump. While switching the diode from direct voltage to reverse one, initially we can observe high reverse current limited mainly by consecutive resistance of the base. This current is caused by accumulated in the base minority carriers. The reverse current saves its value during the time of dispersal (t_{dis}). Later all accumulated in the base carriers pass through the p-n junction or recombine in the diode's base, as a result of which a reverse current decreases to the stationary value – the current of saturation. Renewal of the reverse resistance of the diode ends at this time.

The process of dispersion of the accumulated carriers happens considerably slower than the process of their accumulation, therefore the process of dispersion determines the frequency properties and operating speed of most diodes. For pulse diodes the parameter of duration of reverse renewal of t_{rr} is entered. It is duration of renewal of reverse resistance or current, which is determined by a time domain between the moment of switching of voltage on a diode from a line on reverse one and moment, when a reverse current will decrease to the given value (fig. 2.3, a).

During connecting of diode to the generator of current ($r << Rg$) a current, that passes through a diode, coincides after a form with the pulses of generator (fig. 2.3,). *In* the given mode the pulses of voltage on a diode are examined. At passing of direct current through a diode in the first moment after including there is growth of voltage. It is caused by large initial resistance, which is saved until integrated transmitters will not decrease resistance of base of diode. Therefore, for estimation of fast-acting during connecting of impulsive diodes to the generator of current a parameter is used – duration of direct renewal of diode *of* t_{fr}. It is a time domain, during which

including of diode and direct voltage is on him is set from the value even to the zero, to the set value.



a) b)

Fig. 2.3. Oscillograms of currents and voltages of impulsive diode during his work in the mode of large amplitudes in circuits with the generator of voltage (a) and generator of current (б)

Usually this parameter is fixed at a level, when after the maximal troop landing voltage will fall to the value 1,1 ... 1,2 *U* (fig. 2.3).

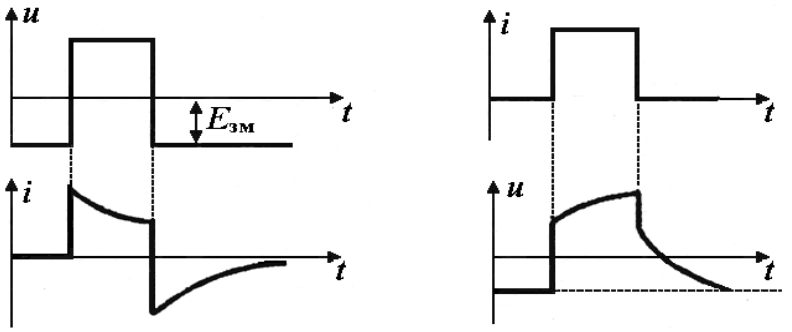
1.3. Junctional Processes at Low Voltage and Current

At the appendix to the diode of small direct voltage (work with the generator of voltages) the effect of modulation of thickness and resistance of base through the low level of injection is very small (fig. 2.4, a). Therefore, resistance of diode has a capacity character. A current passing through a diode sharply increases and limited only by base resistance.

In the process of loading of barrier capacity voltage on *p-n* junction and current through a diode heads for some set values which are determined by the active constituent of resistance of *p-n* junction. In the moment of switching of voltage diode on barrier capacity cannot change instantly, it achieves the set value after some time. The current of diode has the negative troop landing and gradually diminishes (fig. 2.4, *a*).

During connecting of diode to the generator of current in the first moment of action of pulse all current consists of capacity constituent. Therefore, voltage on a diode is determined by falling of voltage on resistance of base of diode (fig. 2.4,).

Voltage on a diode grows in the process of loading of barrier capacity. At the shutdown of diode on him some time is saved remaining voltage which diminishes in course of time (fig. 2.4,), which is determined by the digit of barrier capacity through active resistance of *p-n* junction.



a) b)

Fig. 2.4. Oscillograms of currents and voltages of impulsive diode at his works in the mode of small amplitudes in circuits with the generator of voltage (a) and with the generator of current (b)

To diodes, developed after in 1964 denotation from four elements is given. The first element-letter or number which marks initial material (G or 1 – germanium, C or 2 – silicon, A or 3 – connection of gallium). The second element – letter, that indicates on subset of device (In – varicap, D –universal and impulsive rectifier, Ts – righting posts, blocks and in.); the third element – number the first number of which marks a classification number, and next two numbers (from 1 to 99) – sequence number of development (except stabilitron and voltage regulator diode). To every type of semiconductor diodes the set classification number (varicap – 1,2; righting blocks depending on power – 3,4; rectifier diode of small power (direct current to 0.3 And) – 1, middle power (direct current from 0.3 to 10 And) – 2. Impulsive diodes are classified on duration of renewal of reverse resistance: more than 150 ns – 5, from 30 to 150 ns – 6, from 5 to 30 ns – 7, from 1 to 5 ns – 8; less than 1 ns – 9. For example, CD504A – silicon diode impulsive, in course of time renewal more than 150 ns.

The external environments of diodes are resulted in reference books [4, 8]. It is necessary to memorize that for the rise of reliability the working loading of diodes must not exceed the values higher than 70-80 % maximum possible.

Literature: [1, c. 14 – 39, 44 – 49]; [2, c. 4 – 19]; [3, c. 19 – 44]; [4, c. 94 – 99]; [5]; [7].

2. PROCEDURE

"Researches of semiconductor diodes" execute work by means laboratory module.

1. To familiarize with an of principle electric circuit for research of junctional and frequency parameters of semiconductor diodes, by setting of switches and sockets on the pay (fig. 2.5).

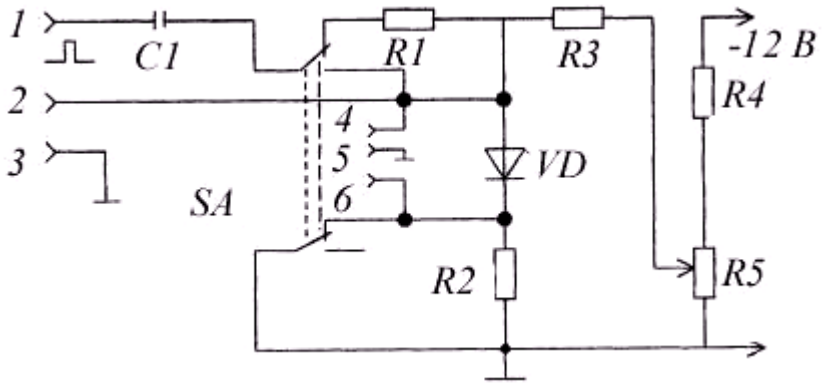


Fig. 2.5. The principle electric circuit for research semiconductor diode

2. To examine junctional processes in semiconductor diodes D226, D223B and D2G with the generator of voltage in the mode of large amplitudes. For this purpose:

– to include the generator of impulsive signals and biradiate oscilloscope;

– to connect the output of generator 1:1 to the outputs of removable pay of *1* and *3* laboratory desk;

– to set by means the buttons and handles of the smooth adjusting such parameters of entrance test signals: frequency – 100 kHz, duration of delay – 0.5 μs, duration of pulses – 0.6 μs, polarity – positive, amplitude – 1,0 V;

– to connect an output to sync pulse of generator to the entrance SYNCHRONIZATION of oscilloscope. To translate a switch SYNCHRONIZATION of oscilloscope in position EXTERNAL and by means the pens LEVEL and STAB obtain the permanent state of tracing of oscilloscope and its absence at are disconnected to sync pulse of generator;

– to connect one output of oscilloscope to the entrance of circuit (terminal *2*) (or to the output of generator), and second – to the output of circuit (terminals 6 and 5 – CORPS);

– to set by a switch TIMEBASE of tracing which will provide the reflection of pulses thus, that oscillogram occupied 1/3 ... 1/4 parts of oscilloscope screen;

– to connect to the pay the diodes D226, D223, D2G and measure duration of dispersal and duration of renewal of reverse resistance of t_{rr};

– to set the class of semiconductor diodes, which diodes D226 belong to, D223, D2G on duration of renewal of reverse resistance.

3. To examine frequency properties of diodes D26, D223 and D2G. For this purpose:

– to include the generator of harmonic vibrations. To set such parameters of sinusoidal vibrations: frequency 200 kHz, amplitude to 1,5 In (to translate a switch in position "1.5");

– to connect the output of generator of harmonic signals to the entrance of pay (to disconnect a cable from the output of impulsive generator and connect him to the output of generator of harmonic vibrations);

– to translate the switch of oscilloscope SYNCHRONIZATION in position of the ITERNAL SWICH oscilloscope SWEEP LENGTH to propose duration of tracing at which in a screen is represented 4 ... 5 periods of entrance sinusoidal signals;

– to connect the second entrance of oscilloscope to the terminal *6*. To translate a switch "SA" on the pay of laboratory desk in position "2". Thus diodes are examined in the circuit of rectifier;

– to draw and define amplitude of positive and negative semiperiods on frequencies 200 Hz, 2 kHz, 20 kHz and 200 kHz. Setting of frequency is achieved by means the switch DIVIZOR OF FREQUENCY of generator;

– to do terminals about possibility of the use of diodes for construction of rectifiers in the range of frequencies 200 Hz – 200 kHz.

4. To examine a diode D223 in the circuit of amplitude limiter. For this purpose:

– to translate a switch "SA" on the pay in position of "1", to connect the second entrance of oscilloscope to the terminal *4* (a terminal IS A *5* CORPS) and by means the potentiometer of the "|**»** second entrance of oscilloscope combine the tracing with the central line of screen oscilloscope;

– to take off dependence of amplitude of positive semiperiod (to deduct from the central line of screen at position of switch of strengthener of the second channel of oscilloscope 0.5 VOLT/DEL). Connecting amplitude of entrance signal in scopes from 0.1 In to 1,5 V. Plot the description $Vvih = f(Vvh)$.

5. To turn off devices.

6. To formulate terminals and design a report.

3. CONTENTS OF THE REPORT

The report must contain:

1. The purpose of laboratory work.
2. The principle electric circuit for research of junctional processes in semiconductor diodes during work in circuits with the generator of current and generator of voltage.
3. The basic parameters of diodes D223 and D226, taken from a reference book, with decoding of their denotation.
4. Oscillograms of junctional processes in diodes during work in circuits with the generator of voltage and generator of current in the modes of large and small amplitudes.
5. Research results as tables and graphs.
6. Terminals based on analysis of the results.

4. QUIZ

1. What parameters of diode as a key, his fast-acting is determined?
2. What the fast-acting of diodes is limited by?
3. By what is determined time of renewal of reverse resistance of diode?
4. Point classification of diodes at times renewal of back resistance.
5. What diodes are named key?
6. Explain the capacitive properties of diodes.
7. Account for the traces of current, which flows through a diode during work with the generator of voltage in the mode of large amplitudes.
8. How does the form of current change that flows through a diode, at the increase of amplitude of entrance pulse and voltage of displacement?
9. Account for the traces of voltage of diode during work with the generator of current in the mode of large and small amplitudes.
10. Why at the increase of frequency of diode are valve properties lost?
11. What processes the limitation of amplitude of pulses is due to?

LABORATORY WORK № 3

STUDY OF VOLTAGE REGULATOR DIODES

The purpose of the work: Deepening and consolidating knowledge about the basic physical processes that occur in reverse-biased p-n junctions, features of semiconductor avalanche diodes, and their performance parameters; acquiring skills of experimental research into such devices and determining indexes of shunt regulators.

1. INTRODUCTION

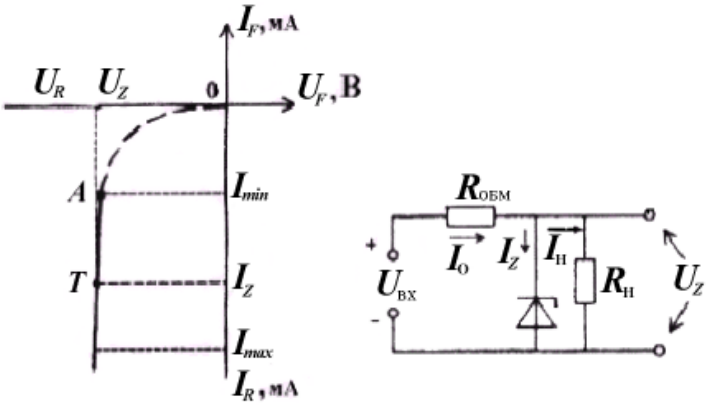
Semiconductor diodes are effectively used even in reverse bias. When reverse voltage reaches a fixed critical value, the diode's current begins to increase sharply. This phenomenon is called diode breakdown. There are two types of breakdown: electric and thermal. A thermal breakdown destroys the device, but electric breakdown is used for semiconductor diodes—in particular, semiconductor voltage regulator diodes. There are two types of electric breakdowns, which quite often accompany each other: avalanche breakdown and Zenner breakdown.

Avalanche breakdown is explained by avalanche multiplication of carriers due to shock ionization and due to the extraction of electrons from atoms by a strong electric field. This breakdown is typical for *p-n* junctions with great thickness and arises at comparatively small concentrations of impurities in semiconductors. The voltage of avalanche breakdown is in the tens or hundreds of volts.

Zenner breakdown is explained by a phenomenon called the tunnel effect. It occurs when a strong electric field with a voltage greater than 10 V/m^2 acts on a thin p-n junction. Some electrons pass through junction without changing their energy. Thin junctions, in which the tunnel effect is possible, are obtained when the semiconductors are heavily doped. The voltage corresponding to Zenner breakdown usually does not exceed a few volts.

The current-voltage characteristic of semiconductor diodes in the region of electric breakdown has an area used for voltage stabilization. Such an area for silicon-junction diodes corresponds to a wide-ranging change in reverse current. Until the onset of breakdown, the reverse current is very small, but during breakdown, such as when stabilizing voltage, it acts like forward current. Currently, only silicon

voltage regulator diodes are produced, but in many different varieties. They are also called voltage-reference diodes because stable voltage received from them is in some cases used as a reference. In figure 3.1(a) a typical *I-V* chart for a voltage regulator diode with reverse current shows that, during stabilization, the voltage changes little. The diagram for forward current in a voltage regulator diode is the same as for ordinary diodes. At point A, where breakdown becomes stable enough, the current increases sharply; the possible value of I_{max} is limited only by its power rating.



a) b)

Fig. 3.1. a – current-voltage characteristic of a voltage regulator diode; *b* – schematic diagram of a shunt regulator

In modern avalanche diodes I_{max} can be anywhere from ten milliamperes to several amperes. The operating voltage of a shunt regulator, which is the voltage potential of the *p-n* junction, depends on the concentration of impurities in the *p-n* structure and is from 4 to 200 volts.

To stabilize low voltage, silicon diodes called forward reference diodes (or stabistors) are used with forward bias. For example, diodes D219C, D222C, and D223C (or, internationally, G129) provide a steady direct voltage of 1 to 1.5 volts (with 50 mA direct current at 25 °C) [3, 4].

Accordingly, to all-Union State Standard 10862-72, voltage regulator diodes were designated in the following way. The first element of the designation defines the basic material: K – silicon. The second is a letter describing the subclass of the devices: C – voltage regulator diodes. The third character in the designation is the power index. The fourth is an encoded designation of the nominal stabilization voltage. The fifth is the order of development (letters of the Russian alphabet from A to Z). Decoding the third and fourth elements of the designation is usually done with the help of a reference book. Let's consider an example designation: KC168A –

silicon semiconductor voltage regulator diode not exceeding 3W of power, with a stabilisation voltage of 6.8 V, of order of development A [3, 4].

The voltage of a voltage regulator diode when operating depends little on the current, which is the reason for using these devices to construct shunt regulators. In the operating region of its I-V characteristic (from I_{min} to I_{max}) the dependence of the diode's voltage on current is described by its differential resistance:

$$r_d = \frac{\partial U}{\partial I} = \frac{\Delta U}{\Delta I}. \tag{3.1}$$

The schematic of a shunt regulator is illustrated in figure 3.1.b. The resistance of limiting resistor $R_{ОБМ}$ must be considerably greater than the differential resistance of the diode. The greater the ratio $R_{ОБМ}/r$ is, the better the voltage stabilisation is.

The voltages and currents in a shunt regulator are connected in the following way (fig. 3.1.b):

$$U_{in} = I_0 R_{obm} + U_z; \tag{3.2}$$

$$I_0 = I_z + I_H. \tag{3.3}$$

Upon increasing the input voltage U_{in}, the output voltage U_z should increase. However, even a slight increase in U_z leads to a sharp increase in the diode's current (fig. 3.1*a*). As a result, I_0 increases and, accordingly, the voltage drop $I_0 R_{obm}$ does too, which compensates U_{vh}'s increase, so the output voltage remains almost constant. Upon reducing input voltage U_{in}, current I_o decreases, and the voltage drop $I_0 R_{obm}$ decreases, which compensates U_{in} instability.

If voltage of the source (the input voltage) is unstable (varying from $U_{\min}$ to $U_{\max}$) but the load resistance R_H is constant, the value of resistor R_{obm} is calculated for the mean point by the formula

$$R_{obm} = \frac{U_{av} - U_z}{I_{av} - I_H}. \tag{3.4}$$

where $U_{av} = 0.5 \cdot (U_{\min} + U_{\max})$ – the mean value of input voltage, $I_{av} = 0.5 \cdot (I_{\min} + I_{\max})$ – the average current through the regulator diode, $I_H = \frac{U_{st}}{R_H}$ – the load current.

The second possible stabilisation state applies when U_{in} is a constant, and R_H varies within the range of $R_{\min}$ to $R_{\max}$. Let us consider as an example the case when R_H decreases, and thus I_H increases. Then the total current in the circuit grows ($I_0 = I_z + I_H$). So, the voltage drop across the limiting resistor R_{obm} increases, and across the diode and load, it decreases. The decrease of voltage on the diode causes

an abrupt decrease in the current passing through it (fig. 3.1*a*). As a result, the input current I_0 and voltage drop $I_0 R_{obm}$ also decrease, and the voltage across the load and diode will remain as before. In this way, the load current growing by ΔI_H automatically causes the current through the diode to drop by ΔI_z. Thus, $\Delta I_{\mathbf{H}} \approx \Delta I_z$, so that $I_0 = I_z + I_H$ is constant. The value of resistor R_{obm} in this case can be determined through the mean values of the currents by the formula:

$$R_{obm} = \frac{U_{in} - U_z}{I_{av} - I_{H.av}}. \tag{3.5}$$

where $I_{H.av} = 0.5 \cdot (I_{H.\min} + I_{H.\max})$, in which $I_{H.\max} = \frac{U_z}{R_{.\max}}$, and $I_{H.\min} = \frac{U_z}{R_{.\min}}$.

The given formulas allow us to choose the right type of avalanche or Zenner diode and to calculate the values of a shunt resistor's elements according to the electrical characteristics and the limits of its operational data given in reference books.

The quality of a constant-voltage regulator work is represented by the stabilisation ratio, K_{st}, which is the ratio of relative change of input voltage to relative change of output voltage:

$$K_{st} = \frac{\frac{\Delta U_{in}}{U_{in.av}}}{\frac{\Delta U_z}{U_z}} \tag{3.6}$$

The stabilisation ratio of a shunt regulator is around 20 to 50.

The performance parameters of a voltage regulator diode are: U_z – stabilisation voltage; $\Delta U_{z\,nom}$ – limit of variation of stabilisation voltage; $I_{z\min}$ – lowest possible stabilisation current; r_d – differential resistance of the voltage regulator diode; and α_{st} – the stabilisation voltage's temperature coefficient.

Literature: [1, pp. 50-53]; [2, pp. 17-19]; [3, pp. 55-58]; [4, pp. 92-94]; [14].

2. PROCEDURE

The work is fulfilled by means of laboratory module 2 "Researches of semiconductor avalanche diodes".

1. To familiarize with the principle electric circuit of parametric stabiliser (fig. 3.2) and location of elements of adjusting on the module board.

Input voltage changes with help of the potentiometer U_{in}, and it is controlled by a voltmeter *PV1*. Restrictive resistance changes with help of the potentiometer R_{obm}. Avalanche diode, that is examined (*VD2)*, is connected to the terminals. It is necessary to check up correspondents of avalanche diode polarity to the polarity of voltages, which acts on the entrance. During the research, the positive voltage is applied to the entrance. In an operating condition the reverse branch of avalanche diode CVC is used, thus to the overhead terminal a negative electrode must be connected.

The current of the avalanche diode is controlled by the millimeter *PA1*, and current of loading – millimeter *PA2*, resistance of loading is changed by means the potentiometer *R9*.

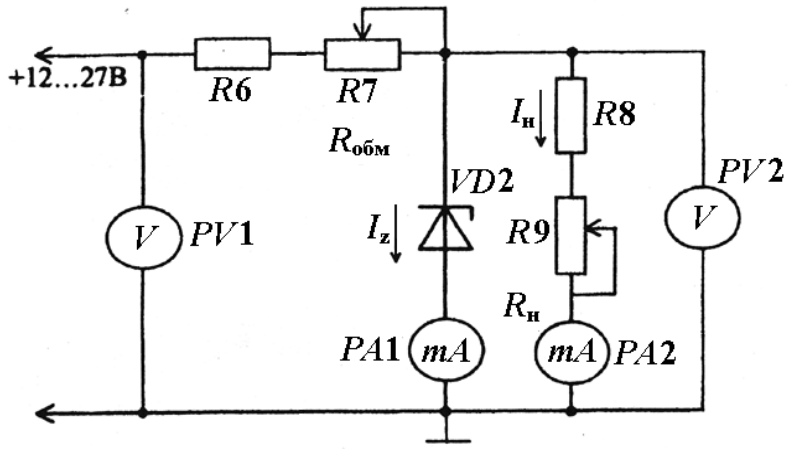


Fig. 3.2. The principle electric circuit for research semiconductor avalanche diode

2. To show out a potentiometer U_{in} in the left extreme position (against an hour-hand), potentiometers R_{obm} and R_H – in middle position. To set the ranges of measuring devices: *PV1* and *PV2* – 200 V, *PA1, PA2* – 20 mA. In laboratory stands with scapiform devices to set the following ranges: PV1 and PV2 – 30 V; *PA1* and *PA2* – 30 mA. To include a laboratory stand (to push the button NETWORK) and voltage source 27 V.

3. Check the capacity of the laboratory set-up. Upon increasing Input voltage, the indexes of all devices must be increased. The currents of the avalanche diode and loading must change at the connecting of position of movable potentiometers indicators R_{obm} and R_H. About the noted rejections in work of laboratory desk to report to the control of laboratory works.

4. Take off the reverse branch of avalanche diode CVC by performing the following actions:

– show out potentiometers R_{obm} and U_{in} in the left extreme position $R_{obm.\min}$, and potentiometer R_H – in right extreme position ($R_{H\max}, I_H \approx 0$);

– smoothly increase U_{in} and, observing after evidence *PV1, PV2* and *PA1*, fix the coordinates of point $AU_{z.\min}$ and $I_{z.\min}$ (fig. 3.1, *a*);

– define voltage on avalanche diodes (U_z) in points VAC $I_{\max} = 18\,\text{mA}$ and $I_z = 0.5 \cdot I_{\max}$. At the increase U_{in}, observe after the correct choice of range of measuring devices. They have not pinning;

– move a potentiometer R_{obm} in right extreme position and repeat described earlier measuring.

5. Note the results of measuring to the table. Build the reverse branch of VAC of avalanche diode $I_R = f(U_R)$ and the graph of dependence $U_z = f(U_{vh})$ at two values R_{obm}. Define these values ($R_{obm.\min}$.and $R_{obm.\max}$).

6. To take off dependence of current of the avalanche diode, current of loading and initial voltage U_z from resistance of loading R_H:

– to set potentiometers R_{obm} and R_H in right extreme position ($R_{obm.\max}$ and $R_{H.\max}$);

– to increase input voltage to the value after which a current through avalanche diode achieves the value $I_{\max}$. To fix the value U_{in} and to support it to constant;

– to fix the value U_z, I_z, I_H in three potentiometer positions R_H at $R_{H.\min}$, $R_{H.\max}$ and one intermediate value;

– to conduct such measuring at the minimum value of restrictive resistance (potentiometer R_{obm} – in the left extreme position). To compare the value U_z at $R_{obm.\min}$.and $R_{obm.\max}$.

7. To turn off the power supplier 27 V and the laboratory stand.

8. To note the results of measuring to the table. To build the graphs of dependence: $U_z = f(U_{in})$ and $I_z = f(U_{in})$, $I_H = f(U_{in})$, $U_z = f(R_H)$, $I_z = f(R_H)$, $I_H = f(R_H)$ at $R_{obm.\min}$.and $R_{obm.\max}$. First, second, third – separately, the fourth, fifth and sixth graphs accordingly to combine.

9. To analyse the results, to make the conclusion and design protocol of the report.

3. CONTENTS OF THE REPORT

The report must contain:

1. The purpose of the laboratory work.
2. Electric parameters, VAC and maximum operating data of avalanche diodes of type CS 522A, that are examined.
3. Denotation and graphic image of avalanche diodes on a standard.
4. Principle electric scheme for researching of avalanche diodes.
5. Results of experimental researches as tables and graphs.
6. Terminals, which are based on the analysis of the results.

4. QUIZ

1. Describe the types of semiconductor diodes disruption.
2. Under what conditions is tunnel disruption possible?
3. What branch VAC in avalanche diodes and stabilisers are working? Why?
4. Draw VAC of avalanche diode and explain principle of action of parametrical stabiliser.
5. How is the stabilisation of initial voltage at reduction of input passing?
6. Why the voltage on avalanche diode does not change at the increasing of load current?
7. How chosen the value of restrictive resistor in a parametrical stabiliser?

LABORATORY WORK № 4

STUDY OF BIPOLAR TRANSISTORS IN STATIC MODE AND IN MODE STRENGTHENING

The purpose of the work: deepening and consolidating knowledge from the fundamentals of the theory of bipolar transistors (BT), study of features of work BT in the modes of small and large amplitudes, acquiring skills and abilities of experimental receipt and research of static characteristic, determination of low-signal parameters and forming of low frequency models. Construction of line of loading, dynamic entrance description and optimum choice of the mode of transistor at strengthening of harmonic signals and pulses.

1. INTRODUCTION

1. Modes of bipolar transistors. BT is contained two interactive electron-hole junctions. Depending on their state (it is opened – closed) four modes are distinguished: active (linear strengthening of signals), pinch-off, satiations and inversions.

a) In the active mode on emitter junction for providing of injection of transmitters of charge in a base direct voltage U_{EB} is given, and on collector junction which carries out extraction of transmitters of charge, – reverse voltage U_{EB}.

A transistor is the guided device. His collector current relies on the current of emitter. It is needed to remember that from the current of emitter substantially that constituent of current of collector depends only, that is conditioned by transmitters, injected from an emitter in a base and pulled in in the circuit of collector.

Degree of influencing of entrance circuit of transistor of emitter – in a circuit with a general base (SB) and base – in a circuit with a general emitter (CE) estimate by means static parameters: coefficient of transmission of current of emitter of h_{21B} or α and coefficient of transmission of current of base of h_{21E} or β. The guided constituent of current of collector in a circuit with a general base is evened αI_E, and in a circuit with a general emitter – βI_B.

b) In the mode of satiation opened both junctions. Collector junction already does not carry out complete extraction of transmitters from a base those results in their piling up intensive recombination. In the mode of satiation the current of base can turn out compared to the current of emitter.

c) In the mode pinch-off, both junctions are closed. The currents conditioned by the processes of thermal generation of transmitters of charge in the volume of semiconductor pass through them, regions of by a volume charge and on the linear contacts, and also currents of effluence.

d) In the inversion mode, emitter junction is closed, and collector – is opened. The current of collector is determined after the value of direct voltage U_{CB}.

2. Static descriptions. The basic descriptions BT take: entrance, that a current and voltage is linked on the entrance; output, that link a current and voltage on an output. Descriptions of transmission, that currents or voltages are linked on an output with currents or voltages on the entrance; descriptions of feed-back, that voltages or currents are linked on the entrance with currents or voltages on an output.

For a circuit with SB entrance descriptions are determined from dependence $I_E = f(U_{EB})$ at $U_{CB} = const$ (fig. 4.1a).

At the reverse voltage increases the current of emitter grows on a collector, entrance descriptions are displaced more left. It is explained by that voltage on a collector affects concentration of transmitters near him and changes the thickness of base as a result of change of thickness of collector junction (expansion of depleted zone). It is the so called effect of modulation of thickness of base.

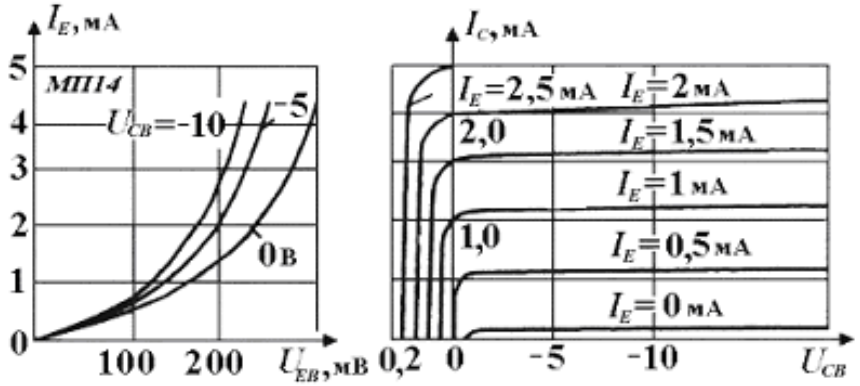
Initial descriptions for a circuit with SB are determined from dependence $I_C = f(U_{CB})$ at $I_E = const$ (fig. 4.1b).

If the current of emitter equals a zero, this dependence presents by itself description of electron-hole junction at the reversed bias. If in the circuit of emitter the created some current, even at zero voltage of collector a current flows in his circuit. At the serve, the direct current of collector junction appears on the collector of direct voltage. So as he flows to the meet to the current of injection, a resulting current with growth of direct voltage quickly diminishes to the zero, after it (at the subsequent rise of direct voltage of collector) acquires reverse direction and begins grows like a weed.

Static descriptions contain complete information about a transistor as an active element of radio electronic circuits. In the mode of large signals, when a working point is displaced on a considerable area, descriptions, they are the basis of grapho-analytical method of analysis and computation of transistor circuits.

In the mode of small signals, a working point is displaced on the small area of entrance and initial descriptions. Therefore, a transistor can be considered as a linear element. In this case, for the analysis and computation linear methods are used. After descriptions of transistor low-signal differential parameters are determined.

3. Differential parameters of transistors. Sizes, that have the small increase of currents and voltages, name the differential parameters of transistor.



a) b)

Fig. 4.1. Static descriptions of bipolar transistor with a general base: a – entrance; b – exit

At presentation of transistor by a linear two-port circuit most practical application is found by three systems: h-, y-, z- parameters.

At the use of h-parameters as independent variables an entrance current is chosen I_1 and initial voltage U_2.

Evening acquire a kind:

$$U_1 = h_{11}I_1 + h_{12}U_2; \quad (4.1)$$

$$I_2 = h_{21}I_1 + h_{22}U_2 . \quad (4.2)$$

From here physical sense and name of h- parameters:

$h_{11} = U_1 / I_1 \big| U_2 = 0$ – entrance resistance of transistor at the short circuit on an output for the variable constituent of current;

$h_{12} = U_1 / U_2 \big| I_1 = 0$ – coefficient of feed-back after voltage at the a secret is broken entrance for the variable constituent of current;

$h_{21} = I_2 / I_1 \big| U_2 = 0$ – differential coefficient of transmission of current;

$h_{22} = I_2 / U_2 \big| I_1 = 0$ – initial conductivity of transistor at the a secret is broken entrance for the variable constituent of current.

The low frequency values of parameters of transistor rely on the circuit of including and are determined after static descriptions. In work [1] there are junction formulas between the systems of parameters. By means these formulas, when known h- parameters, determine y- and z- parameters et cetera.

4. Models BT. For computation of electronic circuits, that contain transistors, represent them by active linear two-port circuit. Thus, properties of transistor at a small signal are described on means equivalent circuits (electric models). Under a model the electric circuit built from linear electric components (resistors, capacities,

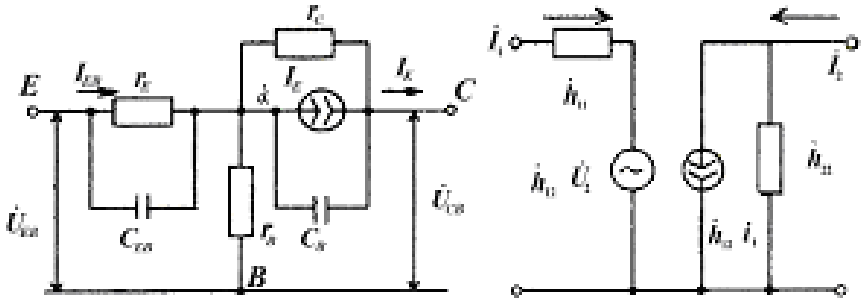
inductances, generators of current or voltage) is understood, that after the properties with a permissible error does not differ from the real transistor.

After a mean the constructions distinguish physical and formal models. Physical models are made on the basis of the physical reasoning for the definite types of constructions of transistors, for a definite frequency range, including of transistor are oriented on a definite circuit (with a general emitter, general base, general collector). Every element of physical equivalent circuit answers the electrode of transistor (fig. 4.2a). The parameters of circuit of substitution of r_E and r_C are considered accordingly as differential resistances of emitter and collector junctions. Resistance of r_B equals the sum of the distributed resistance of base of r_B' and so called diffusive resistance of base of r_B''.

For low-powered transistors the transferred parameters have such values: $r_E = 20\ldots40\,\text{Ohm}$, $r_B = 200\ldots300\,\text{Ohm}$, $r_S = 100\ldots1000\,\text{Ohm}$. In the reference books of value of r_E, r_B, r_C are not usually led, therefore calculate them after known h- parameters transistor [1, pp. 146].

Formal models are built on the basis of transistor description by means evening of two-port circuit. At the use h- parameters model BT can be represented as the circuit, shown on fig. 4.2b.

5. Strengthening of power of electric signals. The mode of strengthening BT is achieved at plugging in the circuit of output electrode (collector or emitter) resistance of loading. In this case the change of entrance signal (for example, change U_{EB}) automatically causes the change of potential on an initial electrode. Terms are characteristic for the static mode ($U_C = \text{const}$) are not executed.



a) b)

Fig. 4.2. Models BT: a – physical; b – by formula

The process of strengthening is characterized by amplification factors: after a current $G_I = I_{vuh} / I_{vh}$ after voltage $G_U = U_{vuh} / U_{vh}$, after power $G_P = P_{vuh} / P_{vh} = G_I G_U$.

For the analysis of active elements in the mode of strengthening the grapho-analytical method based on using entrance and initial static descriptions is widely used.

In a circuit with a general emitter the voltage of collector at presence of loading $R_{C5}(R_5)$ in his circuit $U_{CE} = E_C - R_{C5} I_C$ (fig. 4.3).

This correlation is evening of line. The graph built after her, name description of loading. On family of initial descriptions she is inflicted on to two points: $I_C = 0$, $U_{CE} = E_C$ and $U_{CE} = 0$, $I_C = {E_C}/{R_C}$ (fig. 4.4).

An intersection description of loading with that or other initial static description of transistor is named a working point.

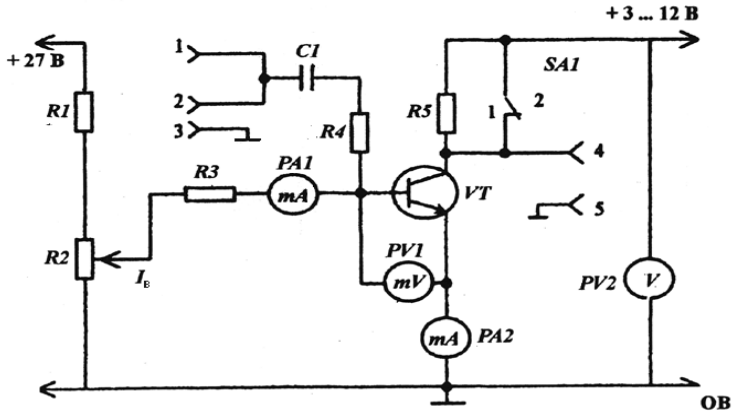


Fig. 4.3. Of principle electric circuit of research BT after a circuit with SE

Entrance description of the loaded transistor differs from static, that it is conditioned by the change of collector voltage. Dynamic entrance description at the increase of current of base consistently crosses family of the static descriptions taken off at $U_{CE} = const$. This description goes more steeply: at the inclusion of loading entrance conductivity of transistors grows.

In the mode of the linear strengthening a working point is chosen into a linear area. Points 1 and 5 on initial descriptions answer the scopes of linear area.

Resulted on fig.4.4 descriptions allow grapho-analytical methods to define amplification factors after a current and voltage (relation of amplitudes of current of collector I_{mC} and current of base I_{mB} and amplitudes of voltages U_{mCE} and U_{mBE}.

Power that is expended by the source of signal on the entrance:

$$P_{vh} = 0.5 U_{mBE} I_{mB} \tag{4.3}$$

Initial power is determined after initial characteristics. The peak value of current on an output is evened I_{mC}, and peak value of voltage on loading

$$U_{mC} = I_{mC} R_C = U_{mC} E. \tag{4.4}$$

Initial power

$$P_{vuh} = 0.5 U_{CE} I_{mC}. \tag{4.5}$$

It is proportional to the area of the shaded triangles (fig. 4.4). Initial power droningly grows in some scopes at the increase of resistance of loading. However because of shunting act of initial capacity of transistor and low complete resistance of entrance circuit of a next cascade of possibility of considerable increase of resistance loading are limited.

The maximal value of amplitude of variable constituent of collector current is limited by the maximum current of transistor ($I_{mC\max} < 0.5 \cdot I_{Cdop}$) the value of which is predetermined by the possible decline of coefficient of transmission of current at the high levels of injection.

The maximal value of amplitude of variable component collector voltage is limited by maximally possible voltage of collector ($U_{mCE\max} < 0.5 \cdot U_{CEdop}$).

Initial power P_{vuh} makes definite part of power that is expended by the source of feed of collector circuit:

$$P_0 = I_{C0} E_C, \tag{4.6}$$

where I_{C0} – current in a working point.

Output-input ratio of collector circuit

$$\eta = P_{vuh} / P_0 . \tag{4.7}$$

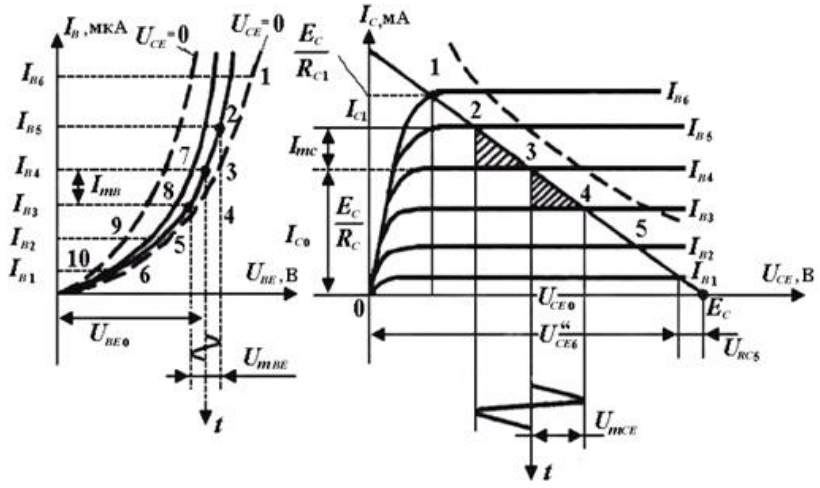


Fig. 4.4. Construction of entrance dynamic descriptions (a) and descriptions of loading for the circuit of including transistor with a general emitter (b)

Other part of power P_C is expended in collector junction on the unavailing heating of transistor.

At strengthening of harmonic and bidirectional pulse signals choose an entrance working point in the center of linear area. It provides maximal amplitude of initial signal: $U_{mCE} = 0.5 \cdot E_C$. If a circuit is intended for strengthening of pulses of positive or negative polarity, for the receipt of maximal initial signal with amplitude, that E_C is evened almost, a transistor in the initial state must be found either in the mode of cutoff, or satiation. The transistors of type of *p-n-p* at including with a general emitter

and general collector are opened at the receipt of negative pulses. Therefore, in this case in the initial state a circuit must be closed (fig. 4.3, point 6).

Literature: [1, pp. 39–41, pp. 56–95]; [2, pp. 19–30, pp. 186-189]; [3, pp. 59-97]; [4, pp. 110-135]; [5]; [8].

2. PROCEDURE

Work is executed by means laboratory module by 3 "Researches of bipolar transistors after a circuit with a general emitter".

1. To familiarize with the of principle electric circuit of the module (fig. 4.3) location on the panel of regulative elements.

Resistors R_1, R_3 and potentiometer R_2 (Current of base I_B) provide displacement of working point of transistor in the active mode. The current of base is controlled by means multimeter *RA1*. Voltage U_{BE} is measured by means the voltmeter *PV1*, and voltage U_{CE} – by means the voltmeter *PV2* (initial range 20 V). A resistor R_5 is loading in the circuit of collector and provides the mode of strengthening, if toggle switch SA1 is found in position "2" (in position of "1" – static mode). Set voltage on a collector by means the potentiometer E_C and control by a voltmeter *PV2* (initial range 20 V).

2. To show out potentiometers in the left extreme position. To translate a switch *SA1* in position "I".

3. Using pin out resulted in reference books, to connect a transistor to the proper terminals of the laboratory module.

4. To include a laboratory stand and sources of feed "27 V" and "12 V ". To check up the capability of laboratory bench by the increase of voltage on a collector (by a potentiometer E_C) and increase of current of base (by a potentiometer I_B). The testimonies of all measuring devices must change. They must not read off-scale.

5. To take off two entrance static descriptions BT at voltages on a collector 0 and at $U_C = 5\text{V}$. For this it is necessary:

– to set voltage on a collector $U'_{CE} = E'_C = 0$ (to turn off a source "12 V");

– connecting by a potentiometer "I_B" current of base and measuring him by means *RA1*, and voltage by a base-emitter – by means *PV1*, to fix the co-ordinates of three points on initial (to the nonlinear area) and three points on a steep linear area. At research of transistors by the КТ201Б potentiometer I_B to set the current of base to 10, 50, 100, 150 μA and fix on the *PV1* proper value U_{BE}. After it, diminishing the current of base, to fix U_{BE}, at which the current of base will begin to equal a zero;

– to include a source "12 V" and by means the potentiometer "E_C" set on a collector U''_{CE} =5 V;

– to take off dependence $I_B = f(U_{BE})$ how described higher.

6. To take results in table and build entrance statistical descriptions for U'_{CE}=0 and U''_{CE}=5 V.

7. To take off three initial static descriptions BT at different currents of base. At research set the KT201Б current of base to such, that is evened 50, 100, 150 μA. It is necessary for this purpose:

– by means the potentiometer "E_C" to set voltage on a collector U_{CE} = 10 V, and by means the potentiometer "I_B" – current of base, that is evened 50 μA. To fix the co-ordinates of point (I_{C1}, U_{CE1});

– to set voltage on a collector U_{CE2} = 7 V and U_{CE3} = 3 V, to fix the co-ordinates of points (I_{C2}, U^{CE2}) and (I_{C3}, U_{CE3});

– to repeat described higher measuring at the currents of base: 100 and 150μA.

8. To take the results of measuring in table and build three initial static descriptions BT.

9. To define differential parameters h_{11} and h_{12}, h_{21} and h_{22} for a working point in the center of linear area by entrance and initial static recommendation BT.

10. To take off the co-ordinates of two points and build the line of loading. It is necessary for this purpose:

– to translate a switch *SA1* in position 1;

– by a potentiometer "*EC"* to set voltage of source of feed E_C = 10 V;

– to the collector circuit (output of circuit of lines. 4.4) to connect an oscilloscope with the opened entrance (switch to "Enter" on the front panel of oscilloscope in overhead position "⎓"); in such mode an oscilloscope allows to measure permanent voltage on a collector;

– attenuator oscilloscope of "Attenuation" switch in position of "2V/sm", handle of the smooth adjusting – in extreme right position;

– to switch a potentiometer I_B in the left extreme position (to set the minimum current of base) – to close a transistor, the current of collector diminishes here, and voltage on a collector aspires to E_C (to voltage of source of feed). Thus, the tracing of oscilloscope is displaced up;

– by a potentiometer "I_B" to set the maximal current of base (150 μA) – it answers the opened state of transistor, potential of collector here to 0 and the tracing of oscilloscope is displaced downward. To fix this level by means the tracing of the second channel of oscilloscope;

– at marked higher position of potentiometer I_B to define by means scale net of oscilloscope of value of displacement of tracing on the vertical line of "Y" sm. At the correct calibrating of oscilloscope equality must be executed 2 V/sm x Y sm = E_C. Position of tracing of oscilloscope of the relatively zero fixed level determines voltage on the collector of transistor. In the closed state U_C = E_C. Thus position of toggle switch *SA1* does not affect position of tracing of oscilloscope;

– by means the potentiometer "I_B" to set U'_{CE} = 5 V (the tracing of oscilloscope is displaced on the middle of the range set higher). To define the co-

ordinates of the first point (U'_{CE} = 5 V, I'_C). The line of loading passes also through a point with co-ordinates (E_C and I_C = 0);

– after the co-ordinates of two points on family of initial static descriptions (p. 8) to inflict the line of loading and calculate the value of resistor in the circuit of collector ($R_C = E_C / I_{C.max}$).

11. To examine BT in the mode of strengthening of harmonic signals. It is necessary for this purpose:

– by means the potentiometer I_B to show out a working point on the middle of linear area of descriptions BT (fig. 4.3, point 3), here on a collector the voltage which is approximately evened $0.5E_C$ is set. The tracing of oscilloscope is displaced on the middle of screen. Use the initial mode BT for strengthening of harmonic and bidirectional pulse signals;

– to include the generator of harmonic signals, to connect him to the sockets *1* and *3* on the pay of the module, that is examined. To connect one channel of oscilloscope to the socket *2*, and second to the sockets *4* and *5*. To sketch oscillograph trace of initial signals on such conditions:

a) at amplitude of entrance signal U_{vhmax}, which provides forming on the output of sine signal U_{vuhmax} without distortions;

b) at amplitude of entrance signal $U_{vh} \approx 1{,}5\ U_{vhmax}$;

c) at amplitude of entrance signal U_{vhmax}, when in the initial state a strengthener is found in the mode of cutoff (fig. 4.4, point 6);

d) at amplitude of entrance signal U_{vhmax}, when in the initial state a strengthener is found in the mode of satiation (fig. 4.4, point 1);

To draw all oscillograph trace under entrance and initial descriptions, and also in co-ordinates $U = f(t)$ under an entrance harmonic signal.

12. To include the generator of impulsive signals and synchronize the tracing of oscilloscope. During work with a generator Г5-54 to set the following mode: to push the button Start, to set frequency of reiteration 100 kHz, delay 1 μs, duration of pulses 3 – 5 μs, polarity ⎍, to connect the output of generator 1:1 (at the pushed button "Ч 0.03") to the sockets 1 and 3 on the pay of the laboratory module.

13. To examine a strengthener in the mode of strengthening of different polarity signals. It is necessary for this purpose:

– to translate a strengthener in the active mode at voltage on a collector in the initial mode $U_C \approx E_C / 2$;

– to give on the entrance of circuit, that is examined, pulses of positive, and then negative polarity, connecting their amplitude so that amplitude of initial pulses measured up E_C/2. To mark the proper points on the line of loading and sketch oscillograph trace, combining them with descriptions of p. 8 and in coordinates $U(t)$.

14. To examine a circuit in the mode of strengthening of unidirectional signals. It is necessary for this purpose:

– by means the potentiometer I_B to close BT and give positive on the entrance, and then – negative pulses. To mark initial position of working point on descriptions of p. 8 and sketch of oscillograph trace;

– by a potentiometer "I_B" to translate a circuit in the opened state (mode of satiation) and do the described higher experiment.

15. To turn off a laboratory stand, sources of feed, generator and oscilloscope.

16. To formulate terminals and design protocol of the report.

3. CONTENTS OF THE REPORT

The report must contain:

1. I sweep works.
2. The electric given and maximum operating data of bipolar transistor, that is examined, taken from reference books [5] (The BT type КТ201Б).
3. The values of h-parameter got during researches.
4. Of principle electric circuit of amplifying cascade at the inclusion BJT with a general emitter, general base and general collector.
5. Formal model BT for h- parameter.
6. Results of researches as tables, graphs (on the standard sheet of format A4).
7. Oscillograph traces, which are built by means initial descriptions and line of loading, and oscillograph trace describing from a screen oscilloscope.
8. Terminals, which are based on the analysis of the results.

4. QUIZ

1. Draw the electric of principle circuits of single-section amplifier on a bipolar transistor with THIS, SB and SC and account for setting of elements.
2. How taken into account the effect of modulation of thickness of base after the presence of resistance in the circuit of collector (in the mode of strengthening)?
3. Why in the mode of small signals for the analysis of transistor cascades is it possible to use h- parameter?
4. What parameters the working area of transistor is limited by on initial descriptions?
5. Why is the grapho-analytical method of computation of transistor circuits used in the mode of large signals?
6. How chosen initial position of working point for strengthening of harmonic and unidirectional signals?
7. Draw the flow diagrams of *n-p-n* and *p-n-p* transistors and account for the process of strengthening of electric signals.

LABORATORY WORK № 5

RESEARCHING TIMING DATA AND TRANSIT TIME PARAMETERS OF BIPOLAR JUNCTION TRANSISTORS

The purpose of the work are: deepening and consolidating knowledge about basic physical processes that determine the operating speed of bipolar junction transistors (BJTs) acting as gates. Acquiring skills and abilities for experimental research of transients in BJTs; the determination of time delay, increasing, resolution, and decreasing, and also the dependence of these parameters from a BJT's mode and the amplitude of the input signal.

1. INTRODUCTION

The transit time parameters and timing data of transistors are determined and examined in cut off and saturation modes. The switching speed is of great importance in determining the operating speed of electronics. This parameter is determined by the processes of accumulation and dissolution of non-equilibrium charge in a transistor's base and collector, and in the emitter and collector junctions.

When used as a switch (or gate), a transistor is in either cut off mode (which is its closed state) or in saturation mode. In the first case, in the collector and base circuits a small reverse current I_{CB0} flows and the voltage at the gate's output (in a CE (common emitter) circuit) the voltage is given as:

$$U_{CE} = E_C - R_C I_{CB0} \approx E_C. \quad (5.1)$$

When supplying the input circuit impulses of direct current of sufficient value, the transistor opens and transitions to saturation mode. The voltage of the collector junction $U_{CE.sat} = E_C - R_C I_{C.sat}$ turns out to be direct. The collector junction opens, and injection of holes (in a *p-n-p* transistor) from the collector into the base begins. Thus, in this case, the holes are injected into the base from both junctions, emitter and collector. In saturation mode, upon increasing the input current I_B, the collector current hardly increases; only the injection of charge carriers from the collector into the base increases, and therefore the nonequilibrium charge of the base increases too. The decrease of the gate's input voltage is found as follows:

$$\Delta U_{vuh} = U_{CE.cutoff} - U_{CE.sat} = R_C\left(I_{C.sat} - I_{CB0}\right). \quad (5.2)$$

The processes of accumulation and dispersal of charges exert a significant influence on the shape of pulses at the output of the gate. Graphs of voltages and currents of a transistor when switching are illustrated in figure 5.1.

In its initial state, a transistor is closed with the help of a source of fixed bias, E_B (fig. 5.1*a*). Upon receiving at the input a rectangular pulse of direct voltage U_{vh} , direct current I_{BE}, whose value is determined by the resistance r_E of the emitter junction and the resistance R_B in the base circuit, flows in the base circuit. Because $R_B >> r_E$, $I_{BE} = (U_{vh} - E_B)/R_B$.

After the pulse ends (the voltage of the emitter junction switches into reverse) the reverse current of the junction, just as for a diode, has a large initial value, limited only by resistance R_B : $I_{BE} = E_B / R_B$. This is because the emitter junction's resistance in the first moment after switching is very small result of the saturation of the base by nonequilibrium charge carriers. As the nonequilibrium charge gets dispersed, the emitter junction's reverse resistance increases, and the current of the base rises to the steady-state value I_{BE0} (fig. 5.1).

For a rectangular pulse with input current $I_{B,}$ a pulse of output current I_C (fig. 5.1*b*) appears with delay t_d, determined mainly by the duration of movement of the injected charge carriers movement to the collector junction. This time delay is determined by the interval of a time between the moment when the input pulse reaches 10 % of its steady-state value and the moment when the output pulse also reaches 10 % of its steady-state value. After the transistor transitions from cutoff to active mode, collector current gradually begins to grow, reaching its steady-state value at time t_r, which is defined by the time interval during which the output pulse increases from 10 % to 90 % of its steady-state value. It depends on the speed of accumulation of nonequilibrium charge in the base and the speed at which the collector capacity discharges. Thus, the total time of a transistor's switching consists of the time delay plus the duration of the current's increasing.

$$t_{op} = t_d + t_r . \tag{5.3}$$

After the base circuit is fed the reverse voltage that closes the emitter junction, the output (collector) current doesn't immediately stop. During some time-duration of dispersion (t_s), it practically preserves its value since the concentration of charge carries in the base near its junction with the collector remains higher than at equilibrium, and, as a result, the collector junction remains open (fig. 5.1 c, d).

Only after the nonequilibrium charge in the collector junction disperses on account of recombination and the holes' leaving from the base does the collector current gradually begin to decrease, reaching the value I_{CB0} after time t_f (the duration of decreasing). During this time, the dispersion of the base's nonequilibrium charge continues and recharging of the collector junction's capacity takes place. The emitter junction can be closed before or after the collector junction, depending on the speed of dispersion of the nonequilibrium charge concentrated near it. The process of accumulation and dispersion of the base's nonequilibrium charge q_B when the transistor switches is shown in figure 5.1 *d*. Accumulation begins after time delay t_d. The charge while t_r is increasing reaches the value $q'_B = Q_{act}$ due to the injection of charge carriers from emitter junction. Than in the saturation mode the charge of base increases due to the carriers' injection from the emitter junction. Later, in saturation mode, the charge of the base grows due to the injection of charge carriers from the collector junction,

reaching the value $q''_B = Q_{act}$. After the dispersion of the base's nonequilibrium charge, after turnoff delay $t_{off} = t_s + t_f$, the charge in the base becomes zero.

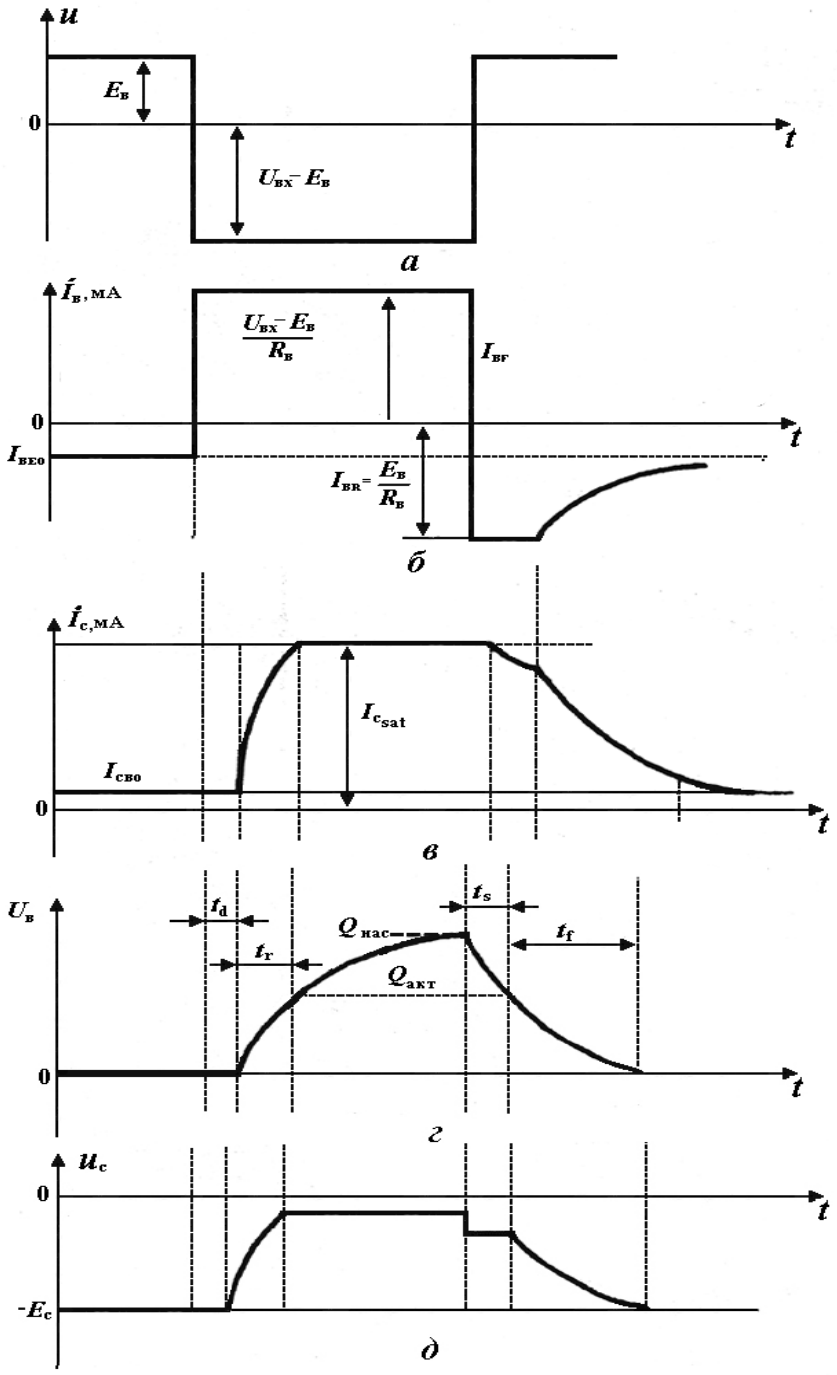


Fig. 5.1. Oscillogram: *a* – input signal; *b* – base current; *c* – collector current; *d* – charge in the base; *e* – collector voltage in a *p-n-p* BJT switch

The magnitudes of t_{op} and t_{off} are determined when evaluating the possibility of using transistors in a device with a given operating speed.

In figure 5.1 e, an oscillogram of the voltage pulse formed on the output of a *p-n-p* BT gate is shown.

One of main problems in increasing the operating speed of gates is reducing the dispersion time of surplus charges. For this, it is necessary to decrease the input signal's amplitude and the base current (fig. 5.1 b), i.e. the degree of saturation, which is ratio of the base current to the saturation base current ($S = I_B/I_{Bsat}$). However, in this case, the duration of the current's increase grows. Additionally, under real conditions the degree of saturation must exceed a minimum value S_{min}. (The value $S = 1$ corresponds to the border with the active mode.) Otherwise the smallest reduction of the current transmission coefficient (β) or the base current will cause the transistor to transition into active mode, which accompanied by an increase in the remaining voltage on the gate.

A universally recognized way to prevent the saturation of a transistor and at the same time avoid the aforementioned complications is to utilize nonlinear feedback in the gate. For this purpose, a Schottky diode is included between the collector and base of a transistor (fig. 5.2).

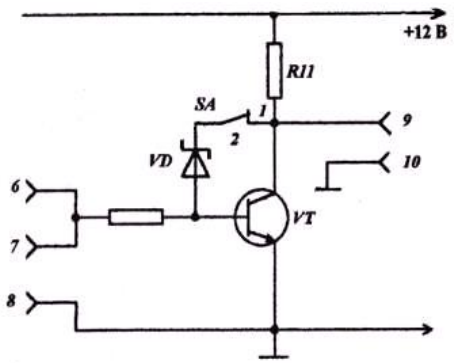


Fig. 5.2. Electrical schematic for studying transient phenomena in a BT with common emitter

When a transistor is closed or working in active mode, the potential of the collector is positive in relation to the base (for *n-p-n* transistors). Consequently, the diode is reverse-biased, has large resistance, and does not affect the work of the gate. When, in the process of forming the leading edge of a pulse, the potential of the collector in relation to the base passes through zero and becomes negative, the diode opens and direct voltage is forms in it. If this voltage is less than 0.5 V (which is typical for Schottky diodes), then the collector junction remains practically closed, and the mode of double injection and accumulation of surplus charge, inherent in the saturation mode, is turned off. As a result, when closing a gate, the stage of dispersion of surplus charge and the delay in decreasing will be absent. The combination of a transistor and a Schottky barrier is known as a Schottky transistor and is widely used in integrated circuit engineering.

It is important to emphasize that, in spite of the absence of saturation, a transistor switch with a Schottky barrier is slightly sensitive to changes in β and the turn-on current, inasmuch as the residual voltage depends a little on these values. The time delay and duration of increasing stay the same as for a saturated gate.

Literature: [1, pp. 92-100]; [3, pp. 99-101]; [4, pp. 135-138]; [14].

2. PROCEDURE

The research of time characteristics and parameters of bipolar transistors at the turning on with CE and CB is executed by means the circuit shown on the front panel of the module 4 “The researches of junctional processes in bipolar transistors” (fig. 5.2 and 5.3). It is necessary to familiarize with the of principle electric circuit of the module and location on the panel of elements of adjusting. To add the transistor, that is examined, to the proper terminals of the module "E-B-C".

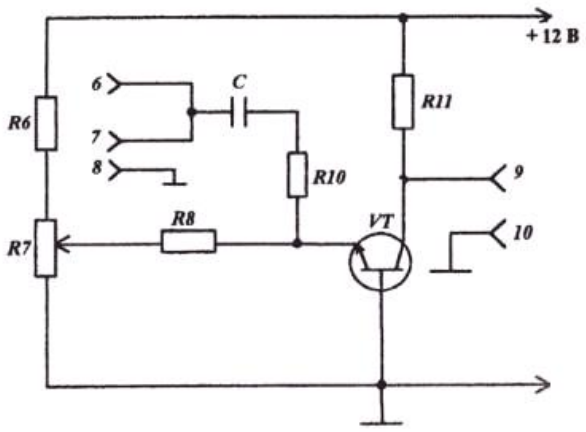


Fig. 5.3. The principle electric circuit for researching transient process in BT with CB

1. To examine the time parameters of the key on BT after a circuit with a common emitter. For this, it is necessary:

– to translate a switch *SA2* in lower position "CE", and *SA3* – in upper position "I";

– to switched on the stand and power supply of 12 V.

2. To switched on an oscilloscope and its entrance AMPLIFIER “Y-II”. Then, connect them to the mortises 9 and 10.

3. To set in position "≃" (the opened entrance after a direct current) switch ENTER on the front panel of oscilloscope.

By a potentiometer “$E_К$”, located in the upper right corner of the module 3, to set voltage on a collector 10 V (the measure is done by an oscilloscope). A transistor must be found in the cut off mode $U_С = E_К$.

4. To fluently revolving the switched on the generator of impulsive signals and its pulses of synchronization, to synchronize trace of oscilloscope. Working with a generator Г5-54 to set the following mode: to push the button START, to set frequency 100 kHz, time displacement – near 1 μs, duration of pulses – 3 ... 5 μs, positive polarity – “_|¯|_”. The test signal turn out through the output 1:1 (at the pushed button " X 0.03"). To connect a generator to the mortise 6 and 8 on the board of the laboratory module.

5. To define the minimum amplitude of input pulse $U_{vh.sat}$, which provides switching of the key in the saturation mode. It is necessary for this purpose:

- amplitude regulator of generator' pulses, to look after the change of signal on the output. In the ascending state the key is in the cutoff mode and $U_C = E_K$. The top of initial negative pulse with increasing of amplitude of input signal approaches a zero level ($U_{Csat} \to 0$). The sign of transferring of the key in the saturation mode is the stability of amplitude of output signal at the subsequent increasing of amplitude of input signal. The top of pulse in the saturation mode achieves a level $U_C \approx 0$ (position of trace of oscilloscope in the case of turn off it entrance from a mortise 9).

6. To measure the time delay of output signal t_d. It is necessary for this purpose:

– to set timebase of oscilloscope 0.1 μs/sm, the handle of the smooth adjusting of timebase to turn clockwise to the end;

– to give on the entrance an pulse with amplitude $U_{vh} = U_{vh.sat}$;

– at the using of single-beam oscilloscope to connect its entrance at first to the mortise 7 and fix position of front with one of vertical lines (to take advantage of handle of horizontal displacement of oscilloscope "↔", or drum of the smooth adjusting of time displacement to lockout pulse of generator). After that to connect an oscilloscope to the output of circuit. Beginning of output pulse will be displaced relatively to the noted vertical line of scale net. Taking into account timebase and size of displacement of output pulse in relation to an input on a horizontal line, determine t_d;

– at the using of dual-beam oscilloscope one input to connect to the entrance of circuit 7, and the second entrance – to the output 9. In a screen at the same time there are two pulses. By potentiometers «↕» to combine them on a vertical line. On displacement of leading edge of output pulse in relation to an input one along the horizontal line, taking into account timebase bit to define t_d. For more clear determination of boards of leading edge of input and output pulses of attenuators of oscilloscope amplifier it is necessary to translate in position 0.2 V/sm and 1 V/sm.

7. To measure the time increasing, dispersal and drop of output pulse at its duration near 3...5 μs. Time of dispersal to measure at timebase bit of oscilloscope 0.1 – 0.2 μs/degree. To displace an pulse in a center of the screen by the pen ↔. To sketch oscillograph trace of output signal, marking levels on the draft E_K and zero potential.

8. To examine the rise of fast-acting of the key by means of nonlinear feed-back. It is necessary for this purpose:

– to connect a diode *VD* between a collector and base of transistor (to translate a switch *SA1* in position "2");

– to give on the entrance an pulse with amplitude $U_{vh}=0.5U_{vh.sat}$. To sketch oscillograph trace and to compare with oscillograph trace, which is got for the given value of amplitude of input signal in p. 7. To compare oscillograph traces of output pulse during connecting and disconnection to the diode *VD* (at switching of switch in position "2");

– to give on the entrance an pulse with amplitude U_{vh} =1,5$U_{vh.sat}$; to define time of dispersal t_s and sketch oscillograph trace of output signal at two position of switch (at the connected and disconnected diode);

– to estimate the increase of fast-acting of the key by means of nonlinear feed-back;

– to turn off the power supply 12 V.

9. To examine the time parameters of the key on a bipolar transistor at the turn on after a circuit with a common base. It is necessary for this purpose:

– to translate a switch *SA2* in upper position "CB", and *SA3* – in position "1";

– to change the polarity of pulse of generator (at research of transistors of *n-p-n* type, in the circuit of emitter a negative pulse is given);

– to show out a potentiometer U_E in the left extreme position ;

– to include the power supply 12 V;

– to measure the intervals of time delay, increasing, dispersal t_s and drop t_f according to the method described in p. 6-7. Duration of input pulses can be diminished to 1 μs, and amplitude must be extended.

10. To compare after fast-acting the key circuits on bipolar transistors with a common emitter and common base.

11. To examine the dependence of amplitude of output signal on voltage of cut off U_E. It is necessary for this purpose:

– to sketch oscillograph trace and define amplitude of output signal at the serve on the entrance of pulses $0.5U_{vh.sat}$, $U_{vh.sat}$ and $1,5U_{vh.sat}$ at three position of potentiometer U_E (two extreme and one middle).

12. To turn off devices, power supply and stand.

13. To formulate terminals, to design the report.

3. CONTENTS OF THE REPORT

The report must contain:

1. The purpose of laboratory work.

2. Oscillograph traces of input signal, current of base, current of collector, unstable charge in a base and voltage of collector in the key on a bipolar transistor with a common emitter.

3. The principle electric circuits of the keys on bipolar transistors with CE and CB for research of transient processes.

4. The results of experimental researches of key circuits on BT as tables and oscillograph traces of output pulses.

5. Terminals that are based on the analysis of the results.

4. QUIZ

1. To call the features of work BT in the key mode.
2. Draw oscillograph traces of pulses on the output of the transistor key with CB and CE.
3. In what way it is possible to promote the fast-acting of the key by a bipolar transistor?
4. How are correlated the duration of increasing in the keys after a circuit with CE and CB?
5. Why does the level of amplitude of input signal do not limited by the value $I_B = I_{Bsat}$?

LABORATORY WORK № 6

RESEARCH OF STATIC CHARACTERISTICS, DIFFERENTIAL AND TIME PARAMETERS OF THE FIELD TRANSISTORS

The purpose of the work: deepening and consolidating knowledge about the field transistors, property of skills of experimental removal – static input and operative (transfer) characteristic, constructions of line of loading and forming of electric models. Determination of differential and time parameters MDS - quadratron KP350A.

1. INTRODUCTION

The field transistors (FT) are unipolar. Their work are based on the use of only one type of carriers – basic (electrons or holes). The processes of injection or diffusion in such devices are practically absent (of principle part is not acted). The basic type of motion of carriers is drift in the electric field.

As and the bipolar transistors and vacuum tubes, FT allow to regulate power, which acts from the power supply in loading. It is achieved by the control of a current through a device due to the change of its resistance. In order to control a current in a semiconductor at the stable electric field, it is needed to change either permittivity of semiconductor layer or its cut. For construction of FT these both methods are used. The field effect lies in the basis of these methods. Leading layer, at which a working current is sent on, is called a channel. Channels are superficial and by volume.

Transistors with a superficial channel make a group of FT with the isolated gate and have a structure: metal – dielectric – semiconductor. They are called the MDS-transistors or MOS-transistors, if in a role of dielectric under the gate an oxide is used (dioxide of silicon).

A transistor with a by volume channel is called the field transistors with operative *p-n* junction.

In spite of unlikeness in a structure, both classes of transistors have following basic characteristics:

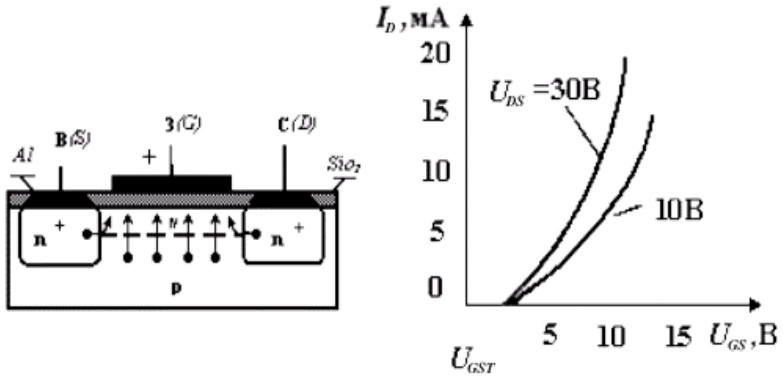
– a handling circuit is fully separated from the operative (initial circuit) and does not practically consume a current, i.e. there is the field operating, and no control by an input current. It predetermines large entrance resistance;

– carried of current is hold true by the carriers of the same sign, that eliminates generation-recombination noises.

In the given laboratory work FT with the isolated gate are research. Two types of such devices are selected: with the induced channel and with a built-in channel. Transistor that is examined to the type KP350A, is FT with a built-in channel and two gates. By analogy with the vacuum lamp devices of they are called MDS- quadratron (four electrodes).

We will consider MDS -transistor with the induced channel of n-type. If in such device to put together a gate (G) with a flow out (S), i.e. when $U_{GS} = 0$ - a channel is absent, and two *p-n* junctions switched in direction to each other turn out on a way between a drainage (D) and flow out (fig.6.1, *a*). At the serve of voltage on a drainage, a current in its circuit will be very small.

At the serve on the gate of voltage of negative polarity $U_{GS} < 0$ near-surface layer will be enriched by the holes. A current in a working circuit changes a little. If on a gate to give greater voltage of displacement $U_{GS} > 0$. the basic carriers of support (holes) will push off from the near-surface layer (a barrier layer expands). Simultaneously the minority carriers are attracted to the surface (in this case electrons). When the growing charge of minority carriers will exceed the charge of majority, the type of conductivity of layer will change.



a *b*

Fig. 6.1. MDS-transistor: *a – the* structure of MDS-transistor with the induced channel; b – transfer (operative) characteristic of MDS – transistor

This effect is called the inversion of conductivity type. After the origin of channel the drainage current takes on an eventual value and relies on voltage on a gate. The subsequent increase of voltage on a gate extends a channel and drainage current is increased. It is operating condition of MDS-transistor. As a current in an entrance circuit is very small, strengthening of power is provided considerably more, than at the use of bipolar transistors.

Leading channels which are absent in the equalibrium state and which appear under the action of external voltage are called induced (resulted by the field to the gate). The voltage on the gate, at which the channel is appears, is called threshold voltage (U_{GST}, its value varies from 1,5 to 10 V). The field transistors with the induced channel are called the transistors of the enriched type. The transfer characteristic of such devices is represented on the fig. 6.1.

The MDS-transistors with built-in *n*- or *p*-channels, which appears in the process of production in the near-surface layer of structure between the regions of drainage and coil (pic 6.2) are created and widely used.

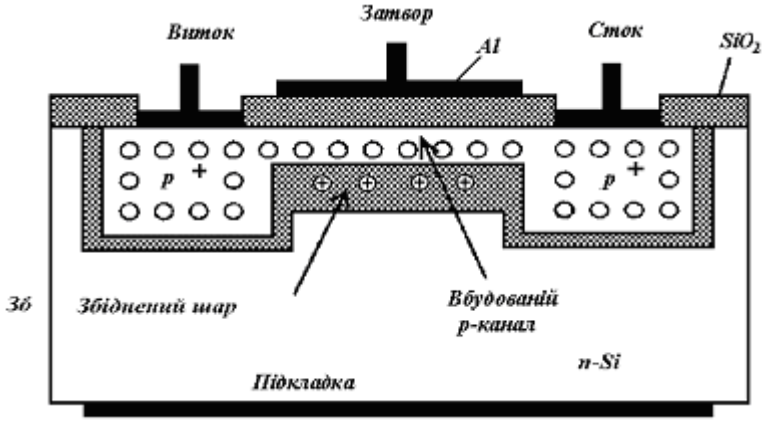


Fig. 6.2. Structure of transistor with the built-in channel of p-type

As a result in such devices a channel exists at zero voltage on gate. Depending on polarity of voltage on a gate a channel can either broaden (mode of enrichment), or narrow (mode of impoverishment). The voltage between a gate and coil, at which the charges of in equalibrium the inversion layer push off from a surface and a built-in channel disappears, is called the voltage of cutoff *(*$U_{GS(off)}$). The field transistors with a built-in channel are called the transistors of impoverished type. The transfer characteristic of MDS-transistor with the built-in channel of n-type are shown on fig. 6.3.

MDS - quadratron is the widespread structural variant of the field transistors. The structure of such device is represented on fig. 6.4. The channel of device is parted on two parts by the heavily-doped region which is called the connecting. MDS - quadratron is possible to depict as two consistently united MDS-transistors. The first gate is operative metallization of which is located above a channel, that connects a flow out and central region. The second gate is called a screen. Operating as an electrostatic screen, it diminishes the value of cross capacitance of device (C_{DS}).

It is extends the range of the stable strengthening of cascade in the region of high-frequencies. In addition, the voltage on the second gate affects common

resistance the drainage –flow out, and thus on the position of transfer characteristic of device. the family of such characteristic is represented on the fig.6.5. The dual-gate FET simplifies the constructing of mixer circuits. MDS – quadratrons experimentally are examined in the given laboratory work.

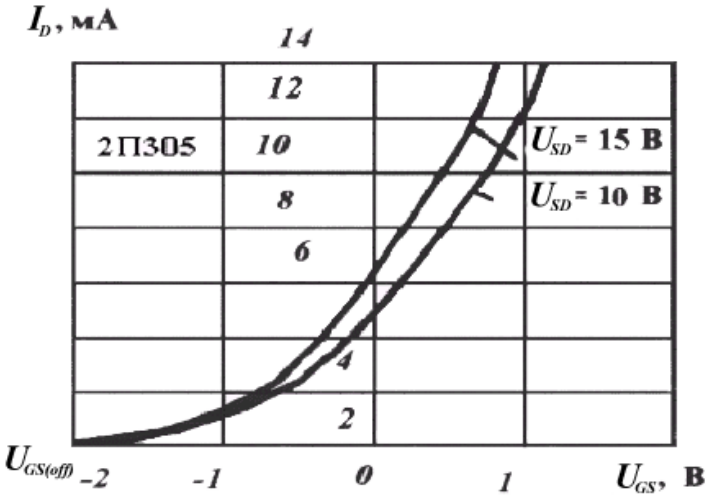


Fig. 6.3. Operative characteristic of MDN-transistor with built-in *n*-channel

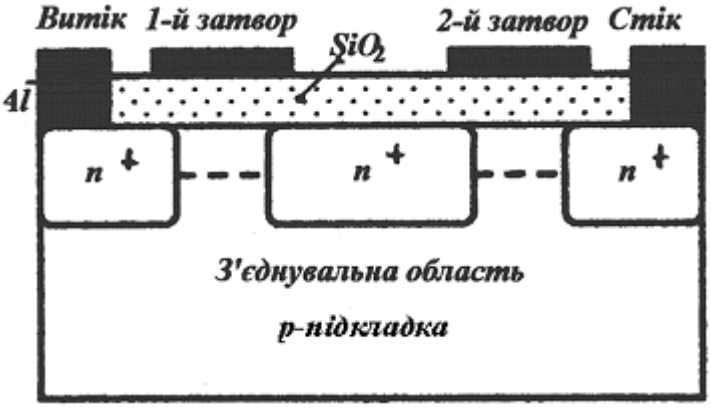


Fig. 6.4. The structure of MDS - quadratron

The most important static characteristic FT are: family of transfer (operative) characteristic $I_D = f(U_{GS})$ at U_{DS} = *const* and the family of initial (drainage) characteristic $I_D = f(U_{DS})$ at U_{GS} = *const*. The operative (transfer or clock-houses) characteristic were considered higher and are represented on fig. 6.1.b, 6.3 and 6.5.

Initial characteristic show that with growth the U_{DS} current I_D at first is increased enough quickly. Then at voltage of satiation $U_{DS.sat} = U_{GS} - U_{GS(off)}$ takes place the reduction of channel, and a transistor passes to the satiation mode. It is explained by that with growth of voltage on a flow out, falling of voltage along a channel is increasing. It predetermines reduction of thickness of channel at approaching to the flow out. When the voltage of flow exceeds voltage of satiation, subsequent growth of current of flow out is stopped, that answers to the horizontal area of initial characteristic of FT, which is called the area of satiation (fig. 6.6).

After the static characteristics the static parameters of the field transistors are determined: steepness *S* (mA/V), internal resistance R_i (kOhm), an amplification coefficient μ. The steepness *S* (conductivity of direct transmission) characterizes of description of operative action to the gate and is determined by attitude of change of current of flow out toward the change of voltage on a gate at the short circuit after an alternating current on the output of transistor in a circuit with a general flow out.

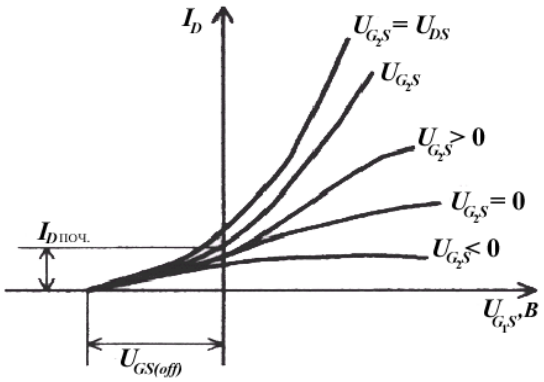


Fig. 6.5.The operative (clock-houses) characteristic MDS- quadratron

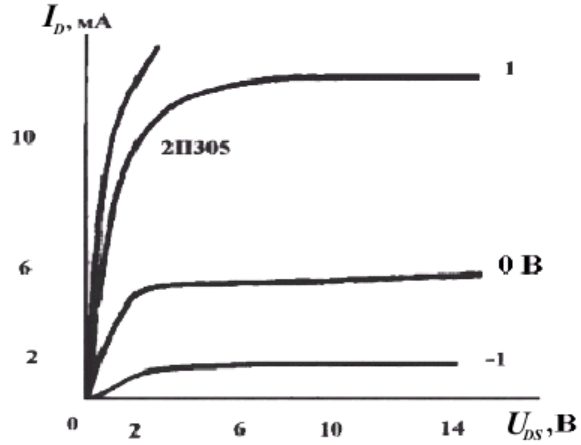


Fig. 6.6. Output (drainage) characteristic of MDN-transistor with the built-in channel of n-type

$$S = dI_{\mathrm{D}} / dU_{\mathrm{GS}} \Big|_{U_{\mathrm{DS}} = \mathrm{const.}}$$

Internal resistance characterizes influence of voltage on the current of flow out

$$R_i = dU_{\mathrm{DS}} / dI_{\mathrm{D}} \Big|_{U_{\mathrm{GS}} = \mathrm{const.}}$$

The static amplification factor μ shows in how many times the stronger the voltage to the gate affects on the current of flow comparatively with voltage of flow out

$$\mu = dU_{\text{DS}} / dU_{\text{GS}} \Big|$$
$$\Big| \; I_{\text{D}} = \text{const}$$

Thus, an amplification factor is $\mu = SR_i$. Alongside with a high amplification factor and entrance resistance the low level of own noises is advantage of the field transistors, firmness to the radiation.

For computation and analysis of electronic circuits with FT, the equivalent circuits (electric models) of such devices are used. It follows to underline that in the mode of small amplitudes, when a working area is located on the small segment of descriptions of transistor, an electronic circuit with FT can be considered as linear. Linear models and linear methods of analysis and computation of electric circuits are used in this case. The field transistor is represented by a model, which is shown on fig. 6.7.

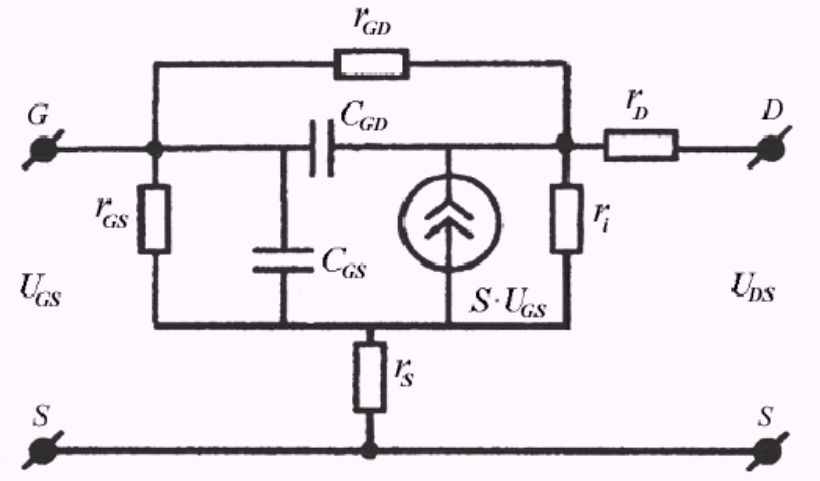


Fig. 6.7. Physical equivalent circuit of FT

In this circuit by an element, to which represents amplifying power of transistor, there is the generator of current SU_{GS}, included parallel to differential resistance of channel *of* r_i. Resistances *of* r_D and r_S present by itself by a volume resistances of semiconductor on areas between the ends of channel and contacts of flow and source accordingly. On low frequencies by influencing *of* r_D it is possible to scorn comparatively with large resistances of loading and r_i. General for entrance and initial circuits resistance *of* r_S is the resistance of internal feed-back FT, switch on after a circuit with a general flow out.

Except for the considered model, formal equivalent circuits are used also, for example with *Y- parameters* (fig. 6.8).

The field transistors, mainly with the induced channel, are widely used as key elements. Known three types of the MDS-transistor keys: with the resister loading, with the dynamic (transistor) loading and complementary keys. Last executed on complementary transistors, that is transistors with the channels of opposite type of conductivity.

Most distribution of parameters were got by a circuit with a general flow out (fig. 6.9), in which operating voltage $U_{IN} = U_{GS}$ is given on a gate, and output voltage U_{out} is taken off from a drainage. The support usually unites with a flow out. On fig. 6.9 the key is represented with the resistance-capacitance coupling on MDS-transistor with induced p-channel, and to that to the circuit of drainage the power supply is included – *ED*.

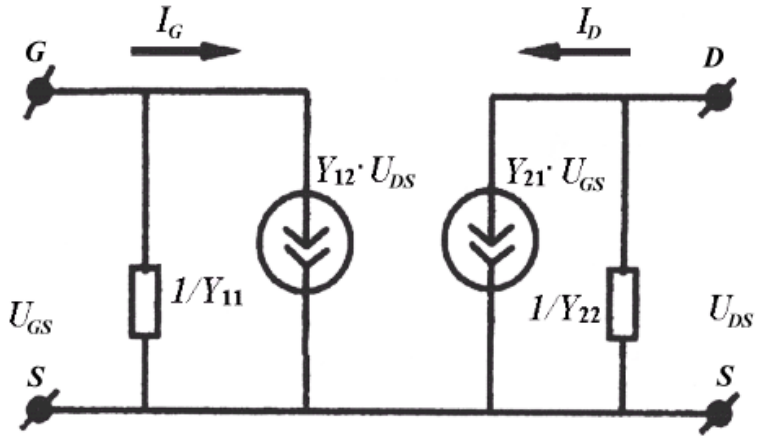


Fig. 6.8. Formal equivalent circuit of FT with Y- *parameters*

The key in an operating mode is found in one of two states (cut off or satiation). In the state of cut off the key is closed, the small remaining current of flow I_{DSX} flows through a transistor. On the line of loading (fig. 6.10) to the closed state of the key a point A is corresponds.

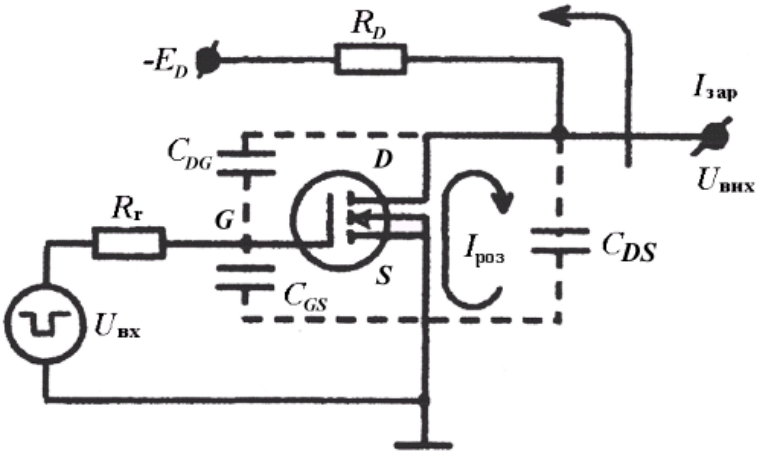


Fig. 6.9. Key circuit on MDS-transistor

In the cut off mode, the input voltage what less than threshold $U_{vh} < U_{GST}$ operates on the entrance. Input voltage closed to the voltage of power supply $U_{vuh} = -E_D + I_{DSX}R_D \approx -E_D$. In the state of satiation the key is opened, a complete current (current of satiation) $I_{D.sat}$ flows through a transistor. A working point B answers such

state of FT that lies on the initial area of input characteristics of FT. In this mode there is entrance voltage more than threshold $U_{vh} > U_{GST}$, and the out put (remaining) $U_{vuh}=U_{rem}= E_D - R_D I_{Dsat}$ diminishes as a result of increase of of voltage drop on loading. Than less in put or remaining voltage U_{rem} in the mode of satiation, than batter the parameters of the key. It follows to underline that of principle limitations on reduction of value U_{rem} in the MDS-transistor keys are not present. Remaining voltage can be done maximum small, increasing resistance R_D and voltage to the gate. However, it follows to take into account that the increase of resistance R_D predetermines the increase of time of switching of transistor from the opened state in closed one. More in detail, it is considered below. If the question of fast-acting of the key is not determining, remaining voltage U_{rem} can be considerably decreased. This one of important advantages of the MDS-transistor keys before bipolar, at which the value of remaining voltage U_{rem} of principle is limited by remaining voltage U_{CEsat}.

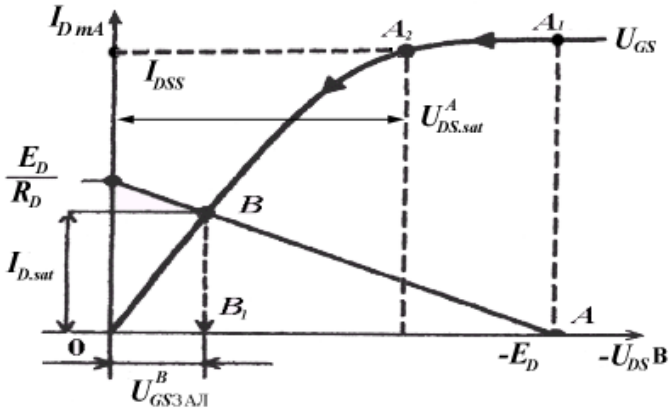


Fig. 6.10. Output characteristic and line of loading key on MDS-transistor

It is necessary to pay attention to denotations and terms. At a bipolar transistor remaining voltage coincides with a term the "voltage of satiation" and is reflected U_{CEsat}. In an arctic transistor by this term the voltage is reflected flow-source, at which input static characteristic becomes declivous, and a current I_D remains almost permanent at the subsequent increase of voltage U_{DS}. It is not a successful term. It does not relate to the mode of satiation, but it is widely used for the analysis of FT.

The opened MDS-transistor than nearer to the ideal reserved key, than less U_{rem}. Thus current of drainage that flows through the opened MDS -transistor, similarly as well as in the key on BT, is practically set by an external circuit (R_D and E_D) and it is called the current of satiation:

$$I_{D.sat} = (E_D - U_{rem}) R_D \approx E_D / R_D . \qquad (6.1)$$

The static state of the opened key is graphically determined on an intersection the CVC loading (lines of loading) and proper input characteristics of MDS-transistor (point B on fig.6.10).

The value of remaining voltage on a transistor must be diminished, in the mode of satiation a considerable current flows through a transistor that predetermines the

large thermal loading on a transistor and considerable losses of energy. Remaining voltage less, than greater steepness of initial area of input characteristics of transistor and greater resistance of resistor R_D. The steepness of the CVC transistor grows at the increase of voltage on a gate. Thus, the resistance of channel diminishes. Typical value of resistance of channel for integral transistors – not less than 1 Ohm, for powerful – tenth parts of ohm. Remaining voltage makes 100 mV and less.

At estimation of possibility of the use of MDS-transistors in the electronic keys their fast-acting which is determined by duration of inclusion and shutdown is important, i.e. by the duration of junctional processes. Such processes must be taken into account, when duration of entrance informative pulses commensurable with duration of junctional processes. Thus the inertia of FT, which is determined by two factors, shows up: by recharging of capacity of gate C_G and recharging of interelectrode capacities.

Influencing of overcharge capacity of gate is taken into account by means of permanent to time steepness τ_S, which represents the inertia FT, conditioned by the gradual change of the operating electric field from a source to the flow: $\tau_S = C_G r_{CHAN}$, where r_{CHAN} − resistance of channel. This parameter is determined only by properties of FT and enabled to set the maximum fast-acting of the keys at the short circuit of circuit of drainage , when it is possible to scorn by influencing of interelectrode capacitances.

At presence of resistance in the circuit of flow the R_D fast-acting of MDS-transistors is usually determined by interelectrode capacities (fig. 6.9), and it is possible to scorn by influencing τ_S through a small size (close 0.01ns). In addition, on the output of the key always there is a total parasite capacity:

$$C_0 = C_{DS} + C'_{GS} + C_{par}, \qquad (6.2)$$

where C'_{GS} − a capacity is the gate-source of the FT of the next key; C_{par} − parasite capacity of editing.

We will consider junctional processes in MDS-key with the resistive-capacity loading. They are conditioned by inertia of FT at the inclusion. That is at switching of the key from the closed state (cut off mode) in the mode of satiation. In the initial state the key is turned off, a transistor is found in the mode of cut off ($U^0_{vh} < U_{GST}$). A capacity C_0 is charged to voltage of power supply, $U_{vuh} \approx \mathrm{E_D}$.

After the serve of rectangular pulse (entrance informative signal) by amplitude $U^1_{vh} > U_{GST}$ (fig. 6.11, a) during duration of delay is formed a new (leading) state of channel. This the time of delay of including of $t_{d(on)}$. It is determined by a time domain between a moment, when an entrance pulse arrives at 10% the set value, and moment, when an output pulse will attain 10% the set value. This process is mainly determined by recharging of capacity to the gate with permanent to time of steepness τ_S. In the general case, there is a $t_{d(on)}$ very brief process (tenth hundredth parts of ns).

Since the conductive state of channel was formed, FT is opened and through a channel flowed current in accordance with amplitude of entrance signal. In our case

the voltage U operates on a gate U_{GS}^{A}, and that the current of flow is set at the level of current of drainage I_{DS}^{A}.

Such process is represented on fig.6.10 by a pointer. The working point of the key passes from a point *A* to the point *A1*. But output voltage U_{DS} through the presence of the charged capacity C_0 can not instantly change. For the digit of this capacity necessary some time. C_0 through the opened transistor runs down by the initial current of flow I_{DSS}^{A}. The voltage on a capacitor, and consequently and on the output of the key falls to the value U_{DSsat}^{A}. A working point is displaced in position *A2*. On the eventual stage of process of inclusion, when voltage on a capacitor will become less U_{DSsat}^{A}, a working point is displaced in position of the B. Current flow diminishes to the level of current of satiation I_{Dsat}, and voltage on the output of the key to the level $U_{rem}^{B} = E_D - I_{Dsat}R_D$.

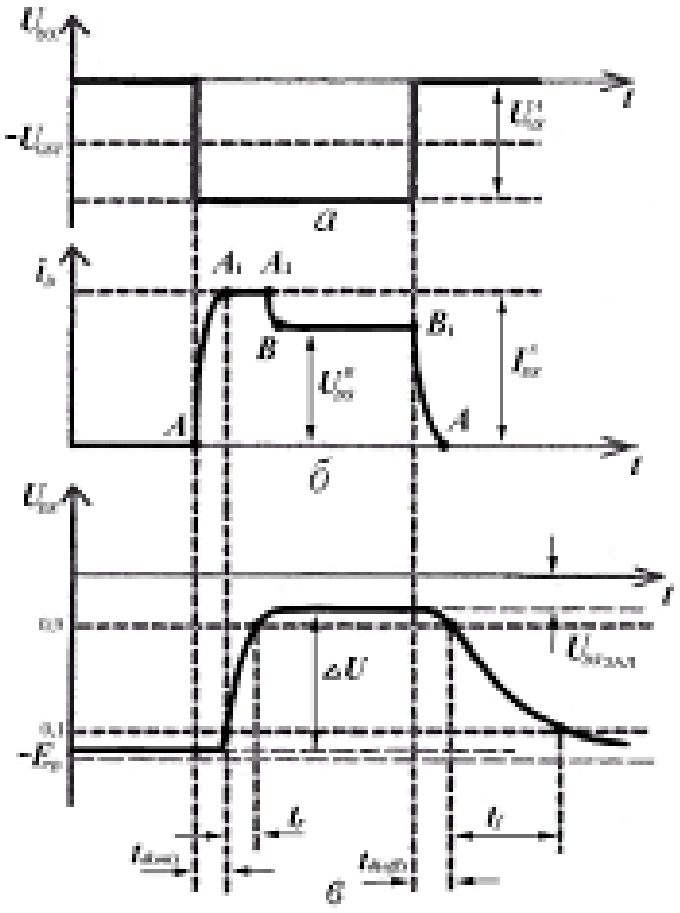


Fig.6.11. Junctional processes in the key on MDS-transistor: *a* – entrance signal; – oscillograph trace of drainage current; *b* – oscillograph trace of input voltage

Duration of including of the keys is determined after a time domain, during which the key passes from the mode of cut off ($I_D \approx 0$) in the mode of satiation (I_{Dsat}). This interval is fixed between the levels of a 10% and 90% set value of current

(see fig.5.1). Taking into account the feature of oscillograph traces of current of drainage on an area A1 – *A2* – *B* (fig. 6.11), we will define duration of growth of current of t_r through the duration of voltage drop (fig. 6.11, b). Duration of voltage drop of FT determines a time domain, during which The voltage on the output of the key falls from 90% to 10% the set value.

Duration of voltage drop on the output of the key can be defined dividing the accumulated on a capacity C_0 charge $E_D C_0$ on the current of digit I_{DSS}^A. We will remind that duration of change of voltage on a capacitor within the limits of 0.9÷0.1 is evened 2.3τ. Duration of voltage drop on an output:

$$t_r = 2.3 E_D C_0 / I_{DSS}^A . \tag{6.3}$$

Complete time of including of the key makes:

$$t_{op} = t_{d(on)} + t_r \approx t_r , \text{ as } t_{d(on)} << t_r \tag{6.4}$$

We will analyze junctional processes in the key on MDS-transistor with the resistive-capacity loading at the shutdown. In the initial state a transistor is opened and on its fallen small remaining voltage U_{DSrem}^B. After action of entrance informative signal $U_{vh}^0 < U_{GST}$ the current of transistor will fall practically to the zero with permanent to time of τ_S and consequently on a flow the voltage U_{DS} is given, $U_{DS} = E_D - I_{DS}^0 R_D \approx E_D$. Duration of this process of $t_{d(off)}$ is conditioned permanent to time of τ_S and is determined as the delay of shutdown. A channel disappears for this time. Through the presence of capacity C_0 voltage U_{vuh} can not instantly change, therefore a working point is displaced pithily B1. The voltage on an output remains at the level of U_{DSrem}^B. The charge of capacity C_0 begins from the power supply E_D through a resistor R_D with constant time $\tau = R_D C_0$. Output voltage grows after an exponential law:

$$U_{DS}(t) = E_D (1 - e^{1/\tau}). \tag{6.5}$$

From here it is possible to define duration of forming of back front of output pulse:

$$t_f = 2.3 R_D C_0 . \tag{6.6}$$

Duration of shutdown of the key:

$$t_{off} = t_{d(off)} + t_f \approx t_f . \tag{6.7}$$

Thus the digit of capacity C_0 takes place through the opened transistor by a considerable current I_{DS}^A, and charge – through a resistor R_D (units of KOhm), therefore $t_{off} >> t_{on}$. distinguishing time is determined by:

$$t = t_{on} + t_{off} \approx t_{off} . \tag{6.8}$$

Such conclusion has a high-quality character, as higher were not taken into account nonlinear of output CVC that considerable change of equivalent capacity C_0 at the change of voltage.

For construction of the keys developed special key FT. The advantages of key MDS-transistors comparatively with BT are: high resistive entrance, that possibility gives to use direct (galvanic) communication between the keys, high fast-acting (duration of switching 1.0.4 ns), connection of high fast-acting with high voltages and currents of switching (to 10 A after 15 ns), small resistance of the opened channel, possibility of parallel inclusion of transistors for the increase of power of switching.

Literature: [1, pp. 111-120]; [2, pp. 30-35]; [3, pp. 114-123]; [5]; [9]; [14].

2. EXECUTION OF THE WORK

Work is executed by means the module of a 6 "Research of FT". For connecting of this module to translate a switch *SA3* in position "*2"*. In work are examined to the FT type KP350A with two isolated gates and n-channel. Executing work is necessary in such sequence:

1. To familiarize with the of principle electric circuit of the module (fig. 6.12) and location of elements of adjusting on its board:

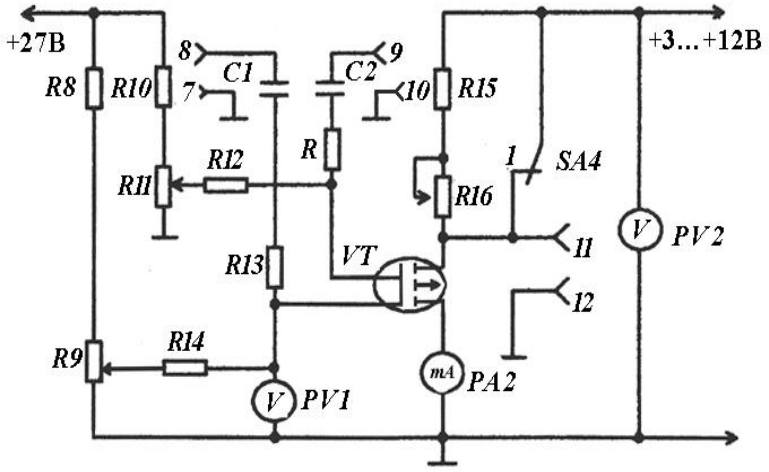


Fig. 6.12. The principle electric circuit of the module for research of FT

For the feed of circuit of drainage use the voltage source 12 V. The voltage is regulated from 3 to 12 V by a potentiometer E_C and measured by a voltmeter *PA2*. Current, that flows through a transistor, milliamperemeter *PV2* is measured, which is plugged in the circuit of source. On fig. 6.12 the represented circuit for research of FT with two isolated gates. The voltage on the first gates regulated by means of the potentiometer *R9* (on a front panel there is the marked U_{31B}) and measured by a voltmeter *PV1*. The voltage on the second gate is regulated by a potentiometer *R11* (U_{32B}). A switch SA4 disconnects loading while conducting researches in the static mode (position "1"). A potentiometer R16 (on a panel there is the marked R_C) regulates resistance in the circuit of drainage.

2. To take off family operative (transfer) characteristic of the field transistor $I_D = f(U_{31B})$ at $U_{DS} = const$ and $U_{32B} = const$. For this purpose:

– to translate potentiometers *R9* (U_{31B}), *R11* (U_{32B}), R_C and E_C in the left extreme position, and U_a – in extreme right (it is located on the module *5*);

– to translate a switch *SA4* in position "1";

– to include the power supply + 12 V and + 27 V and potentiometer E_C, to set voltage of flow 5 V (*PV2* is controlled);

– to translate a potentiometer *R11* in middle position and fix the current of source (flow) $I_B = I_C$ at $U_{31B} = 0$;

– increasing the positive voltage on the first gate by a potentiometer *R9*, to fix the value of voltage U_{31B} and current of flow I_D in three points on an initial growing area and in three points on the declivous area of description;

– to repeat measuring at extreme right position of potentiometer *R11* (when the voltage on the second gate about 12 V);

– to conduct measuring at voltage on a flow 12 V (it is set by a potentiometer E_C);

– to enter results in the minutes and build family of control descriptions.

3. To take off family of initial descriptions FT $I_D = f(U_{DS})$ at $U_{31B} = const$ and $U_{32B} = const$. For this purpose:

– to set on the first breech-block $U_{31B} = 0$ and to translate a potentiometer *R11* in extreme right position ($U_{32B} = 12V$); to fix the current of flow (I_D) at voltage on a flow 3; 5 and 12 V;

– to execute the same measuring at U_{31B} 1 and 2 V;

– to enter results in the minutes and build family of initial descriptions.

4. To define static differential parameters (S, R_i, μ) transistor which is examined, to build the low-frequency electric model (equivalent circuit) of transistor.

5. To build two lines of loading and define the value of resistance in the circuit of flow at the two position of potentiometer R16. For this purpose:

– to translate a switch *SA4* in position of "2", and potentiometer *R16* – in the extreme left position;

– to include an oscilloscope and connect him to the outputs (11 and 12);

– by a potentiometer *EC* to set voltage of feed 10 – 12 V (*PV2* is controlled);

– on family of the initial descriptions built in p. 3, to inflict the point of line of loading with co-ordinates E_D, $I_D = 0$;

– at extreme right position of potentiometer *R11* to set voltage $U_{31B} = 2$ V;

– to define the current of satiation I_{DSsat} (*PA2*) and by means the oscilloscope – remaining voltage on a flow U_{DSrem};

– on sat of initial descriptions to inflict a point I_{DSsat} and U_{DSrem} and conduct the line of loading (it follows to take into account that this point must be found on static description $I_D = f(U_{DS})$ at $U_{31B} = 2$V);

6. To enter the results in the protocol and draw two oscillograph traces. To account for the change of form of pulse and flow and its displacement on a vertical line at the change of value R_C;

– to inflict oscillograph trace on family of output static characteristics with the lines of loading, which are got in p.5;

– to represent the change of form of output signals at the change of voltages on the first and second gates.

It is necessary to pay attention to that on fig. 6.11 oscillograph trace for FT with p–channels are resulted, and in the laboratory work, FT is examined with n–channels.

7. To examine FT at the management by different informative signals which simultaneously will be connected on both gates:

– to include the generator of harmonic signals. Signals by amplitude about 2 V, by frequency 100 to give kHz on the entrance 8 – 7 (body). It is necessary to pay attention to that in the circuit of the module 6 the changes are borne. Unlike a circuit which is represented on a front panel, outputs 8 and 9 are not united between itself. The module which answers a circuit is used (fig. 6.12);

– to add the generator of impulsive signals to the terminals 9 and 10 (second gate) and give negative pulses with frequency 10-20 kHz;

– regulating voltage on the gates of transistor and amplitude of entrance signals, to get the modulated vibrations in screen of oscilloscope. To draw oscillograph trace s at different voltages on gates and two extreme positions of potentiometer *R16*. To account for the results.

Strengthening of sin signals with minimum nonlinear errors is the optimum mode. In order to look after the form of harmonic output signals, it is necessary to translate the switch of oscilloscope SYNCHRONIZATION in position “Internal. 1”.

8. To turn off a stand, power supply, generators and oscilloscope.

9. To analyse the results, to formulate terminals on work and design protocol of the report.

3. CONTENTS OF THE REPORT

The report has to contain:

1. The purpose of laboratory work.

2. Passport parameters of examined FT (KP350A) given and operating, and conditional graphic images and denotation FT.

3. Electric circuit of the laboratory module for research of FT, executed on a standard, of principle.

4. Results of research FT, which are given as tables, graphs, electric model and oscillograph trace.

5. Terminals, which are based on the analysis of the results.

4. QUIZ

1. Draw structures of FT with induced and built-in by channels.
2. Draw and account for operating (transfer) characteristic of FT.
3. How must one define differential parameters FT on family of output characteristic?
4. Draw the low-frequency electric model of the FT and explain the setting of its elements.
5. What are properties of FT inertia and frequency conditioned by?
6. How does the value of resistance in the circuit of flow on remaining voltage and time parameters FT influence?
7. Draw the electric circuits of the MDS-transistor keys of principle with loading resistive and dynamic.

LABORATORY WORK № 7

RESEARCH OF STATIC CHARACTERISTICS AND PARAMETERS OF DIGITAL INTEGRATED CIRCUITS

The purpose of the work: Deepening and consolidating knowledge about the features of digital integrated circuits (DIC) as components of modern electronics, and acquiring skills of experimentally obtaining and researching transmission characteristics and measuring the basic static parameters of a DIC 7400 (155ЛА3).

1. INTRODUCTION

An integrated circuit (IC) or microchip is a set of several interconnected components (transistors, diodes, condensers, resistors, etc.) closely packed together and made simultaneously in one substrate that executes certain transformations of electric signals and, from the point of view structural and technological requirements, is examined as one whole.

The group method and planar technology form the foundation of integrated circuitry, mastered in transistor electronics.

The essence of the group method is that, on a silicon (or germanium) plate with a diameter of 25 to 40 mm, all of the elements necessary for the construction of a functional node are made simultaneously. In order to wire the elements by means of metallic strips, it is necessary that the terminals of all components be located in one plane, on one surface of the plate. Planar technology provides for this, and thus, photolithography is widely used.

Differing in their means of production and use, there are semiconductor, film, hybrid, and monolithic integrated circuits.

A semiconductor IC is a microchip whose elements are connected at the near-surface layer of the semiconductor substrate using special technological methods.

A film IC is a microchip whose elements are formed by different types of membranes applied to the surface of a dielectric substrate. Depending on the way in which the films are applied, integrated circuits are classified as thin-film (up to 1 to 2 μm) and thick-film (10 to 20 μm and more). Such technology does not allow us to obtain active elements in the form of transistors, so film ICs are comprised only of passive elements. Such circuits supplement discrete components mounted onto to them to produce a hybrid IC (HIC). Besides diodes and transistors, the mounted components can also be semiconductor ICs, i.e. components of higher functional complexity.

Monolithic ICs are also used. They are microchips on which there are active elements in the near-surface layer of semiconductor crystal (as with semiconductor ICs) and passive elements in the form of film layers on a previously isolated surface of the same crystal.

In all types of ICs the interconnection of the elements is carried out by means of thin metallic strips etched or drawn to the wafer (the substrate's surface) and at the necessary places for contacts with attachable elements. The process of applying these connecting strips is called deposition, and the wiring image is called the pattern.

There are two different classes of semiconductor ICs: bipolar ICs and MIS ICs. The characteristic feature of such circuits is their lack of such components as inductance coils and, moreover, transformers.

The functional complexity of an IC is characterized by the degree of integration, that is, by the quantity of elements (or transistors) on a chip. For quantitative evaluation, we sometimes use the coefficient $K = \lg N$, where K represents the degree of integration, and N is the number of circuit elements.

Inasmuch as an IC, like a vacuum tube or transistor, presents itself structurally as a unified whole, performs a certain function, and must meet certain requirements upon testing, delivery, and usage, it belongs to the category of electronic devices. However, IC is qualitatively a new type of device.

The first and main feature of an IC as an electronic device is that it independently executes an often very difficult function, while discrete electronic devices execute a similar function only in combination with other components.

The second important feature if an IC is that increasing its functional complexity compared with discrete devices is not accompanied by worsening any of the basic indices (reliability, costs, and so on.). In fact, all these indices improve.

The third feature lies in the preference for using active elements over passive ones. In an IC, the cost is set not on an element, but a chip. Therefore, it is best to put on a chip as many elements as possible with minimal area. Minimal area is achieved using active elements.

The fourth feature is that adjacent elements are located at a distance of only 50 to 100 μm from one another, which ensures that the variation of parameters between adjacent elements is small.

Depending on their functional settings, ICs are divided into two basic categories: analogue (AIC) and digital (DIC).

Analogue ICs are those intended for the transformation and processing of signals that change according to some continuous function.

A DIC is a microchip with the help of which signals expressed in binary or some other digital code are transformed and processed. Such circuits are also known as logical circuits. Such logical elements, or logical valves, perform the simplest logical operations: negation, logical addition, and logical multiplication.

The simplest logical function, negation (also called inversion or the NOT function) is realized by means of an inverter, or NOT gate (for example, by a

transistor switch using a common emitter circuit). The conventional symbol for a NOT gate is shown in figure 7.1 а.

Logical addition (also called disjunction or the OR function) is defined in the following way: $C=1$ if $A=1$ or $B=1$, or $A=1$ and $B=1$. (These letters were shown in the figure before its Ukrainization.) In this case, an output signal is formed upon the arrival of an input signal at either of the gate's input terminals. The symbol of an OR gate is shown in figure 7.1 б.

Logical multiplication (also called conjunction or the AND function) is defined in the following way: $C=1$ if at the same time $A=1$ and $B=1$. In this case, an output signal is created only at such times when there are signals at all inputs. The symbol of an AND gate is shown in figure 7.1 в.

The combination of the OR function and inversion (fig. 7.1 г) provides the combined function NOR. Similarly, the combination of the AND function with inversion (fig. 7.1 д) results in the combined function NAND. Such functions allow us to realize any logical operation.

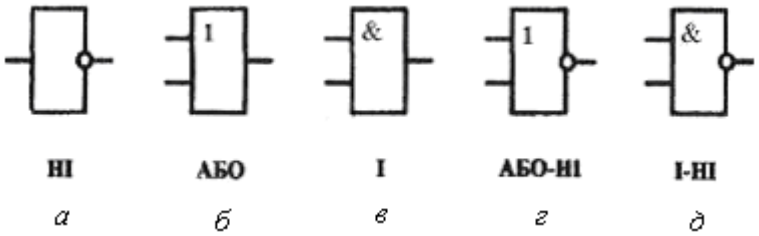


Fig. 7.1. Conventional (though I don't see how because the IEC "rectangular" standard requires "≥1" in the place of "1" on OR and NOR (with "=1" they become XOR and XNOR respectively) and "1" on NOT, and the American "military" form is quite different) representation of basic logical elements

In logical elements, logical zeros and ones are represented by different values of voltage: a low voltage level U^0 (log. 0) for zero and high voltage level U^1 (log. 1) for one. The difference between the levels of one and zero is called the logic swing.

Series of bipolar DICs produced by the electronics industry are divided according to the types of their basic electronic gates into the following families: resistor-transistor logic (RTL), diode-transistor logic (DTL), resistor-capacitor transistor logic (RCTL), transistor-transistor logic (TTL), and emitter coupled logic (ECL). In these titles, the word "logic" represents the notion of an electronic gate.

Along with bipolar circuits, ICs with MOS (metal-oxide-semiconductor) structures became widely used (on P-channel transistors, complementary MOS circuits (CMOS), and so on). The most widespread in modern electronics are TTL, TTL with Schottky barriers (Schottky TTL), ECL, integrated injection logic (I2L), and MOS circuits.

The basis of TTL circuits is made up of multiple-emitter transistors (METs), which are collections of several transistor structures that share a common collector. A simple NOR circuit based on a MET is shown in fig. 7.2.

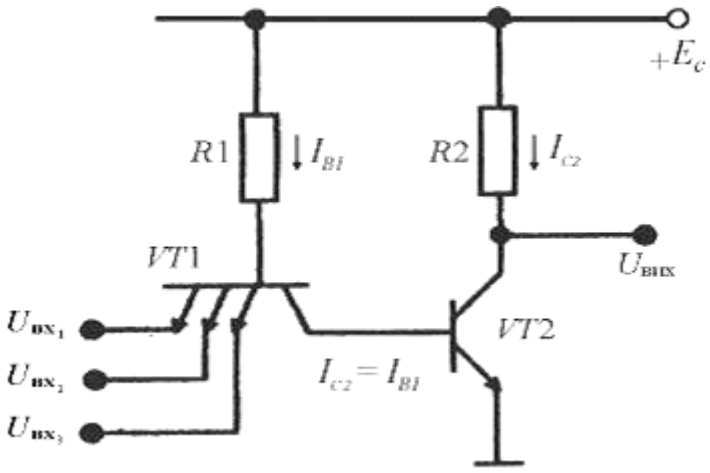


Fig. 7.2. Circuit of a logical element based on a MET

If, on all inputs of the MET (VT1), there is a voltage corresponding to the level of logical “0”, all base-emitter junctions shift forward. A large current I_{B1} flows through resistor R1; the potential of the base diminishes; the collector junction of the MET closes ($I_{C1} = I_{R2} \approx 0$). This ensures that transistor VT2 is closed ($I_{C2} \approx 0$), and at its output the voltage equals the level of logical “1”. If a voltage corresponding to level “1” is applied to one of the inputs while the others retain level “0”, the state of circuit will not change, since the opened emitter junctions of the MET will shunt the closed one and the collector junction. The collector junction of the MET will remain closed.

The output signal will change only during the simultaneous input on all MET emitters of voltage at the level of logical “1”. In this way, the emitter junctions of the MET are all closed, and the collector is opened (inverted mode of the transistor). The current applied to the base of the MET through resistor R1 flows from the power supply to the collector circuit and then to the base of transistor VT2, which transitions into saturation regime. The voltage at the output of the circuit corresponds to level “0” (U_{vh}). In this way, the NAND logic operation will be achieved.

TTL circuits with simple inverters did not find wide use because of their high noise, small load capacity, the slow action of the unipolar gate when working at capacity load, and rigid requirements for the parameters of the integrated elements. For TLL ICs, a gate with a complex inverter—a bipolar gate, which is used to construct the TTLs of standard series 7400 (K155 in the USSR)—is basic. Such logical elements are examined in the given work.

Dynamic parameters of DIC are examined in laboratory work 8.

The system of DIC static parameters is the set of parameters characterized by currents and voltages at all input and output terminals and at the power supply terminals. Measuring the parameters is carried out for the states of log. 0 and log. 1 for each terminal. Static parameters characterizing DICs are conventionally divided into classification parameters, measurable parameters, and mode parameters.

Those not directly measured are classification parameters, and they are supplied by the system of measured parameters and mode parameters or calculated using them.

These include the branching coefficient K_{bra} at the output, the merger coefficient K_{mer} at the input, the noise stability U_{ns}, and the power consumption.

The branching coefficient of the output (load capacity) characterizes the number of inputs of similar circuits that may be connected to the output of the gate. The merger coefficient of the input determines the maximum number of entrances DIC inputs.

The static noise stability of logic gates determines the value of voltage that can be given on a gate's input relative to the level of "0" or "1" without causing erroneous operation. Since a logical gate in static mode is in one of two states ("0" or "1"), we distinguish static noise stability at level "0" (U^0_{ns}) and at level "1" (U^1_{ns}) (see fig. 7.3). Other parameters defined in this way.

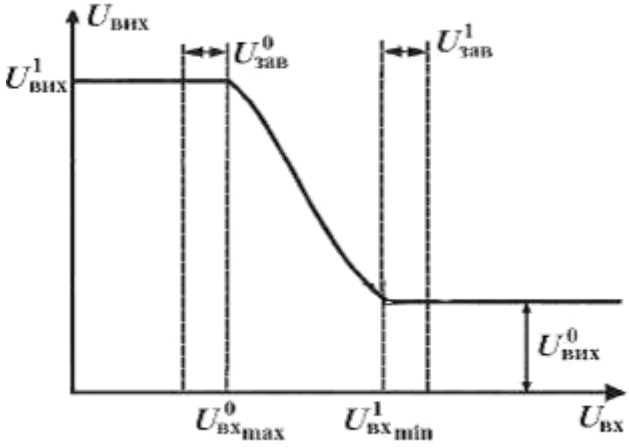


Fig. 7.3. Transmission characteristic of a DIC

Among the most important static parameters of a DIC are: power consumption in the state of logical zero $P^0_{spo}(P_{CCL})$; power consumption in the state of logical one $P^1_{spo}(P_{CCH})$; mean power consumption $P_{spo.c}(P_{CCAV})$, determined as the half-sum of the powers consumed by the microchip from the power supply in two different test states; input voltage $U^0_{vh}(U_{IL})$ and output voltage $U^0_{vuh}(U_{OL})$ of logical zero; input voltage $U^1_{vh}(U_{IH})$ and output voltage $U^1_{vuh}(U_{OH})$ of logical one; input current $I^0_{vh}(I_{IL})$ and output current $I^0_{vuh}(I_{OL})$ of logical zero; input current $I^1_{vh}(I_{IH})$ and output current $I^1_{vuh}(I_{OH})$ of logical one; and threshold voltages of logical one and logical zero (U^1_{por}, U^0_{por}) (the largest value of low level voltage and the smallest value of high level voltage at the input of the microchip at which the chip still doesn't transition from one logical state to another).

Measurement of the static parameters of an IC is conducted at certain points of input, output, and transmission characteristics corresponding to logical levels 0 and 1. The set of reference points for characteristics and parameters derived from them constitutes the system of static parameters of specific IC or an IC series.

The methods of measuring static parameters of an IC reduce to measuring voltages and currents at its output terminals on the condition that, at all outputs of the

circuit being checked, the necessary levels of voltages and currents, i.e. the required electrical mode of the circuit, are set.

In production of ICs, and also in companies utilizing ICs, automated systems for measuring IC parameters are widespread. In this case, programmable test sources controlled by digital signals are used.

Terms, definitions, letter designations of electrical parameters of ICs, and also methods of measuring them used in science and engineering are established by a series of state standards [11, 12, 13].

According to the accepted system of conventional designations, all domestically produced ICs are divided according structural-technological implementation into three groups: 1, 5, 6, 7 – semiconductor ICs; 2, 4, 8 – hybrid ICs; 3 – other (film, vacuum, ceramic and so on.). These numbers are the first elements in conventional designations of ICs. The second element is three digits (from 000 to 999) or two digits (from 00 to 99), specifying the sequence number of a series of microchips. The third element is two letters corresponding to the IC's subgroup and type according to its function (generators of harmonic signals – ГС, universal trigger – ТВ, differential amplifiers – УД, and so on). Sometimes at the end of the conventional designation a letter which determines technological variation of electrical parameters of a given part type is added.

Integrated microcircuits are produced in cases and in caseless versions.

Literature: [1, pp. 120-124; 130-136]; [2, pp. 39-77; 224-234]; [3, pp. 143-153], [4, pp. 154-163; 204-219]; [6]; [11]; [12]; [13]; [14].

2. EXECUTION OF THE WORK

In the given work, the integrated circuit of 155ЛА3 by means the module of a 7 "Research of static descriptions and parameters dis" is examined. It is necessary to execute work in such order.

1. To familiarize with the electric circuit of the module (fig. 7.4) and placing of elements of adjusting of principle. The module connected to the power supply 27 V however for the feed IC is given voltage 3 – 5,5 V, which is set by a potentiometer, that is reflected on a panel U_{dzh}. For measuring of this voltage a voltmeter *PV1* and eliminator of voltage *R1* and *R2* is used. Resistances of resistor *R1* and potentiometer are the *R2* levels. Therefore at extreme right position of handle of potentiometer *PV1* will show 0.5 U_{dzh}. A switch *SA1* serves for the simultaneous serve of entrance signals on both entrances of circuit And or for connecting milliamperemeter *RA1* to the entrance circuit. By loading of circuit, which is examined, the same circuit which is connected through a switch *SA2* serves. Initial voltage is measured by a voltmeter *PV2*.

2. To translate a potentiometer *R2* (U_{vh}) in extreme right position, to include a stand, power supply +27 V. With help of potentiometer U_{dzh} and voltmeter *PV1* to propose the voltage of power supply of microcircuit pursuant to passport data. At

research of the integrated circuit С155ЛА3 U_{dzh}= +5 V. After establishment of voltage is a potentiometer *R2* (U_{vh}) to translate in left extreme position.

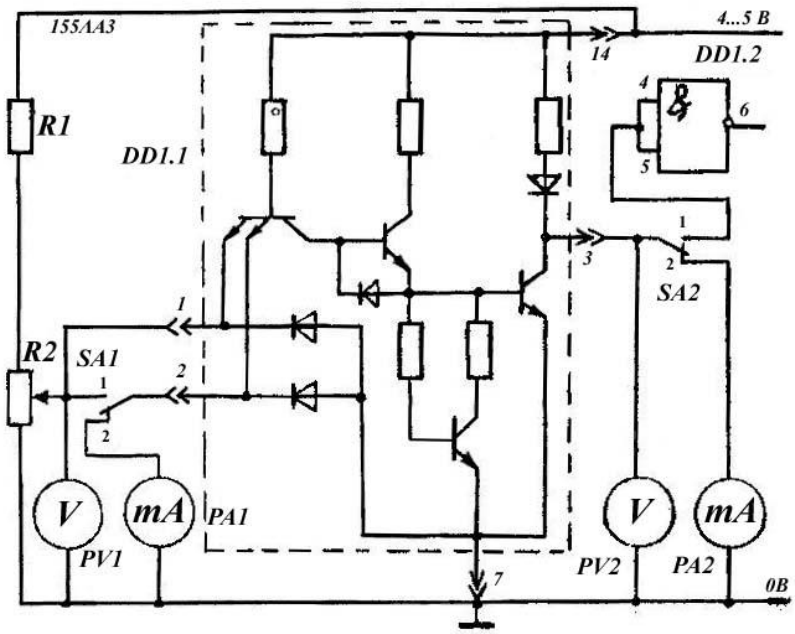


Fig. 7.4. Circuit of the laboratory module for research of static parameters dis

3. To connect loading to the integrated circuit which is examined, for what to translate a switch *SA2* in position “1”.

4. To measure output voltage of logical zero U^0_{vuh}. For this purpose on the incorporated entrances DIC 1 and 2 (to translate a switch *SA1* in position “1”) to give voltage $U_{vh} > U^1_{por}$, that is achieved by the rotation of potentiometer *R2* clockwise to junction of circuit in the opened state. The voltage U^0_{vh} is fixed by means the voltmeter *PV2*. To enter the results of measuring in the minutes of the report.

5. To measure output voltage of logical item U^1_{vuh} and entrance current of logical zero I^0_{vh}:

– on an output, that is examined, to provide the high level of voltage by presentation on the entrance of a 1 voltage U^0_{vh} (a potentiometer *R2* is set U_{vh}=1,5 V in left extreme position);

– to fix the value of voltage of logical item by means the voltmeter *PV2*;

– to measure the milliamperemeter *RA1* entrance current of logical zero of entrance 2, for this purpose to translate a switch *SA1* in position 2; to enter results in the minutes of the report.

6. Experimentally to find transmission description DIC $U_{vuh} = f(U_{vh})$:

– to translate switches *SA1* and *SA2* in position “1”;

– connecting entrance voltage by a potentiometer *R2*, to define an area U_{vh}, which causes the sharp change U_{vuh};

– on the mentioned area to fix the four – five points U_{IN} and U_{vuh};

– outside this area to mark on two points which answer $U_{vh} < U^{0}_{por}$ and $U_{vh} > U^{1}_{por}$, and also to take into account the results of measuring of p. 4 and 5;

– to add the results of measuring to table and build transmission description.

7. Using the method laid out in p. 1, by means the potentiometer U_{dzh} to decrease voltage of source of feed to + 4 In and to repeat the experiment of p. 6. To build transmission characteristics.

8. To measure the current of short circuit on an output I_{kz}:

– to translate a switch *SA2* in position "2";

– on an output, that is examined, to provide the high level of voltage, for what on association to give the entrances the voltage U^{0}_{vh};

– to fix by means milliamperemeter *RA2* the current of short circuit, to enter a result in the minutes of the report.

9. To turn off the power supply and stand.

10. To analyse the results, to formulate terminals on work and design protocol of the report.

3. CONTENTS OF THE REPORT

The report has to contain:

1. The purpose of laboratory work.
2. The graphic image is conditional, electric circuit and static parameters of integral microcircuit of 155ЛА3 of principle that is examined, taken from a reference book from the integrated circuits.
3. Circuit of the laboratory module for measuring of static parameters dis.
4. Results of researches of static parameters dis, given as tables and transmission characteristics.
5. Terminals, which are based on the analysis of the results.

4. QUIZ

1. Draw a circuit dis, which is examined, and explain realization of logic operations, of principle AND – NOT and OR – NO.
2. Explain features IC as a new type of electronic devices.
3. Transfer basic advantages of the use of digital IC.
4. How digital IC does classify?

5. Transfer base functional elements.
6. Compare the parameters of the base electronic keys on bipolar DIC and MOS-structures.
7. Transfer and give determination of basic static parameters dis.
8. What is essence of methods of measuring of static parameters DIC in?
9. Draw transmission description of dis.

LABORATORY WORK № 8

RESEARCH OF DYNAMIC PARAMETERS DIGITAL INTEGRAL MICROCIRCUITS

The purpose of the work: deepening and consolidating knowledge about a structure, principle of action, features and basic dynamic parameters dis, executed on КМОП-transistors, property of skills of experimental determination of basic dynamic parameters to the DIC type K561LA7.

1. INTRODUCTION

Properties of integral logical elements (ILE) in the mode of switching are estimated by means dynamic parameters, which determine after the reaction of circuit in time on action of entrance signals. It is time correlations between signals an input and output, and time diagrams of different modes robots IC.

The following parameters belong to dynamic (fig. 8.1):

$t^{1,0}(t_{TLH})$ – duration of junction IC from the state of logical item in the state of logical zero. This time domain, for which voltage on an output IC changes from the level of log. 1 to the level of log. 0, measured at level 0.9 and 0.1 or on the set values of voltage;

$t^{0,1}(t_{TLH})$ – duration of junction IC from the state of log. 0 in the state of log. 1. It is a time domain, for which voltage on an output IC changes from the level of log. 0 to the level of log. 1, measured at level 0.1 and 0.9 or on the set values of voltage;

$t^{1,0}_{delay}(t_{DHL})$ – duration of delay turn off IC. It is a time domain between an entrance and weekend by pulses at the change of voltage on an output IC from voltage of log. 1 to voltage of log. 0, measured at the level of 0.1 or at set level of voltage;

$t^{0,1}_{delay}(t_{DHL})$ – duration of delay of shutdown IC. It is a time domain between an entrance and weekend by pulses at the change of voltage on an output IC from the level of log. 0 to the level of log. 1;

$t^{1,0}_{delay.distr}(t_{PHL})$– duration of delay of distribution of signal at including IC. It is a time domain between an entrance and weekend by pulses at the change of voltage on an output IC from the level of log. 1 to the level of log. 0. measured at the level of 0.5 or on the set values of voltage;

$t^{0,1}_{delay.distr}(t_{PLH})$ – duration of delay of distribution of signal at the shutdown IC. It is a time domain between an entrance and weekend by pulses at the change of voltage on an output IC from the level of log. 0 to the level of log. 1, measured at the level of 0.5 or on the set values of voltage;

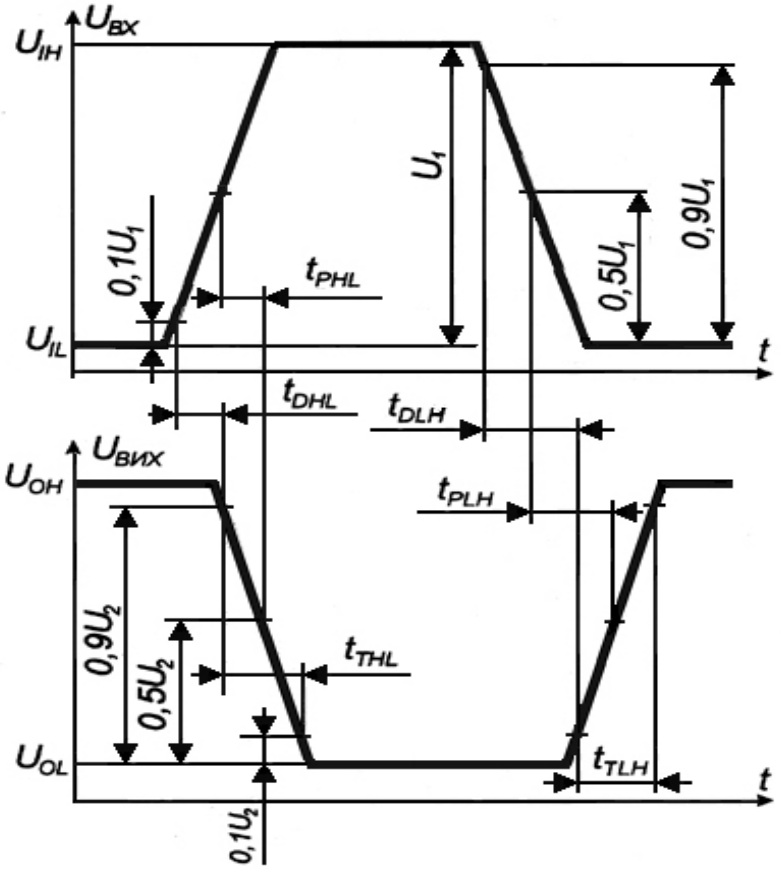


Fig. 8.1. Dynamic parameters DIS

$t^{0,1}_{delay.distr.c}(t_{PAV})$ – means time of delay of distribution of signal of logical IC. It is a time domain, which equals the semisum of time of delay of distribution of signal at the inclusion and time of delay of distribution of signal at the shutdown of logical IC:

$$t^{1,0}_{delay.distr.c} = 0.5\left(t^{1,0}_{delay.distr} + t^{0,1}_{delay.distr}\right). \quad (8.1)$$

Mean time of delay of distribution determines the fast-acting DIS. It value in nanoseconds for different series IC is given in table 1.

Limitations after the fast-acting, what characteristic for p-cannel MOS-circuits, liquidated by means n- cannel MOS-structures. Mobility of electrons in silicon is more than mobility of holes that provides speed of switching of MOS-circuits with n-cannels in 2-3 times more than circuits with p-cannel. Use of method of ionic implantation and structures with poor, instead of with the enriched channels allowed

to lower voltage of feed to 5 V, that does these circuits compatible after electric levels with TTL.

Table 1. Time of distribution delay of the DIS

Type of logic	p-MOS	CMON	TTL	ESTL	n-MON	IL^2
t_{PAV}	100	15 – 50	1 3	0.5 – 2	40 – 100	5

Have the row of important positive qualities elements of injection logic IL2, which appeared as a result, of improvement of technology and circuit technique IC.

The methods of measuring of dynamic parameters DIS are based on determination of time interval between two different (or identical) levels of voltage of signals an entrance and initial. The generator of impulsive signals and measuring device of time intervals use to that end. In this laboratory work is used measuring of time domains an oscilloscope.

At measuring of dynamic parameters as loading a microcircuit and its equivalent is used.

In logical circuits the MDS-transistors are used with an oxidizing dielectric SiO_2 – MOS-transistors. The MOS-transistor keys-inverting lie in the basisc of MOS-transistor logic (MOP TL). In the keys with the dynamic loading transistors are used with the channel of the same type, as well as in active transistors. It is DMOS-transistor logic on the keys of one type of conductivity.

On transistors with the channels of opposite type of conductivity the complementary keys which make the basis of KMOS logic or KMOS TL are executed.

Absence of current in an entrance circuit is the feature of integral logical elements on MOS-transistors. As a result logical even U^O and U^1 does not rely on loading and remain the same, as well as at idling. Influencing of a next key results only in the increase of initial capacity of given logical to the element.

On fig. 8.2 two typical variants of ILE MOS-logic, executed on MOS - transistors with n-channels, are represented. The use of the dynamic loading diminishes an area ILE and extends one of basic advantages MOS TL – high degree of integration. This advantage is conditioned to those, that MOS-structures do not need the special isolation between ILE, unlike a structure on the basis of bipolar transistors.

Transistors VT1 and VT2 are active, and transistors T3 – by the dynamic loading. A gate VTZ is connected with a flow, therefore, $U_{\text{z–v–3}} = U_{\text{s–v–3}}$, that is $U_{\text{z–v–3}} - U_0 < U_{\text{s–v–3}}$ (U_0 – threshold voltage). It means that VTZ works on a declivous area. If on gate VT1 and VT2 (fig. 8.2, a) to give voltage the $U_{vh}^0 < U_0$ transistor VT3 passes to the opened state, its remaining voltage had and $U_{vuh}^1 = E_C$. If on a gate VT1 or VT2 to give voltage $U_{vh}^1 < U_0$ (or on both gates), a transistor (or both) passes to

the opened state, remaining voltage had and $U_{vuh}^{0} \to 0$. Voltage of feed is fully applied to the loading transistor VT3 turned off. For reduction of remaining voltage in the key with the dynamic loading transistors VT1 (VT2) and VT3 must substantially differ. At the active transistor of relation of width to length of channel must be how it is possible greater, and at loading – how it is possible less.

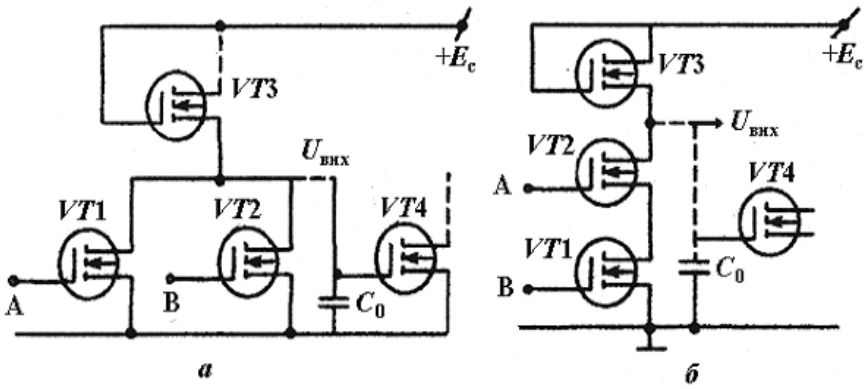


Fig. 8.2. Logical elements MON TL with the dynamic loading: *a* – execute a logic function OR – NO; b – execute a logic function And – NO

Transistors VT1 and VT2 (fig. 8.2, and) are included parallel, washing of each of them off results in reduction of initial level, that is a circuit executes a logic function 2 OR – NO. At the geometry of transistors marked higher remaining voltage has the same small value (0.05...0.15 V), as well as in the bipolar keys. Therefore, it is possible to count $U_{vuh}^{0} = U_{rem} = 0.1\text{V}$.

In a circuit MOS TL remaining voltage diminishes proportionally amounts of the opened logical transistors, so as parallel connection of transistors is attitude of width balanced to the increase toward length of channel.

Usually voltage of feed in MOS TL is elected in 3-4 times greater than threshold voltage. Therefore, if $U_0 = 1.5\ldots3\text{V}$, a logical overfall $(5\ldots10\text{V})$ far exceeds the value, incident to the circuits DTL, TTL and IL2.

Promoted firmness is another advantage MOS TL. For opening of transistor voltage near to the threshold is needed, that is $1.5\ldots3\text{V}$, in that time as in bipolar ILE she makes $0.7\ldots1.4\text{V}$.

It is represented on pic 8.2, ILE differs by the successive inclusion of logical transistors. Therefore current in a circuit and low level of initial voltage U_{vuh}^{0} are possible only at opening of all (in this case both) logical transistors. It takes place at the serve of level U_{vh}^{1} on all logical entrances. Resulted ILE executes a function 2 And – NO. Level U_{vuh}^{1} in the given circuit the same, as well as in previous, but level

U^0_{vuh} anymore – he proportional to the amount of the consistently included logical transistors and can make 0.2...0.5 V and more. According to less there will be a logical overfall.

The fast-acting MON TL is limited to speed of recharging of capacity $C_0 = C_{CV} + C_{ZV} + C_M$ (stray wiring capacitance). Such ILE less fast-actings, than bipolar.

Logical elements on the complementary keys are shown on fig. 8.3, a and b. Basic advantage of CMOS logic is in that the change of output voltage is unconnected with the change of current of flow: he remains near to the zero. As a result of CMOS logical elements consume very small power. In structures CMOS TL parallel connection of one type of transistors is accompanied by successive connection of other type. A logic function, that is executed, is determined by the inclusion of transistors of the "ground" floor. Transistors VT1 and VT2 – transistors with induced n-channel (enriched type), and VT3 and VT4 – with induced p-channel.

If in a circuit (fig. 8.3, *a*) on both logical entrances given low even $U^0_{vh} < U_0$, VT1 and VT2 are closed (channels are absent). Channels so as voltage appear in transistors VT3 and VT4 $U_{z-v} = E_C$ and exceeds (after the module) threshold voltage. However, as insignificant currents of the closed transistors VT1 and VT2 flow through channels, falling of voltage on the channels of transistors VT3 and VT4 goes out small. Therefore it is possible to consider that entrance voltage equals voltage of feed $U^1_{vuh} = E_C$. A logical overfall makes accordingly $U_{vuh} = E_C$.

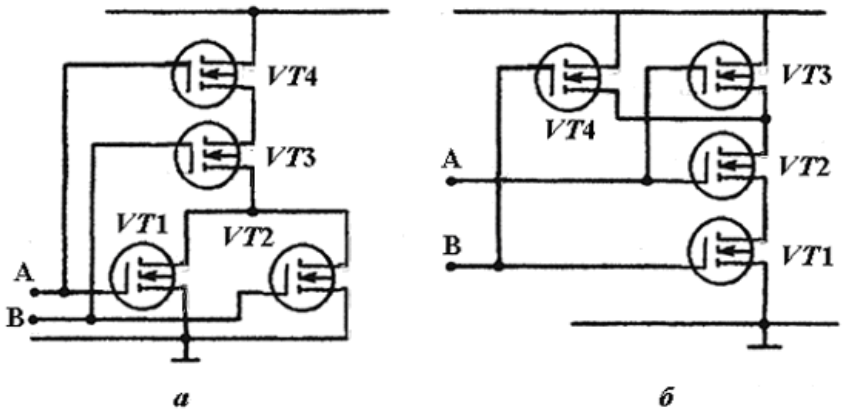


Fig. 8.3. Logical elements CMOS TL: *a*– execute a logic function OR – NO;
b– execute a logic function And – NO

We will consider the case, when an entrance informative signal $U^1_{vh} > U_0$ is given only on one entrance A. This will provide switching of transistor VT1 in the opened state. It is necessary to pay attention to that for the normal functioning ILE on

the basis of KMOS-structures, the level of entrance signal must be such, that a condition was executed $\left(E_C - U_{vh}^1\right) < U_0$.

Then switching of transistor VT4 is provided in the closed state and on an output the level of logical zero will be formed. The same processes take place, if to give U_{vh}^1 only on the entrance B or on both entrances simultaneously.

Initial voltage ILE changes at the serve of level U_{vh}^1 on any of entrances (A or B) or on both entrances. Such element executes a logic function OR – NO.

The state of circuit (fig. 8.3,) changes only at the serve of level $U_{vh}^1 > U_0$ simultaneously on both entrances. Thus a logic function will be realized And – NO.

Except for a high economy, small working voltages are additional advantages CMOS TL on comparison with MOS TL (to $2U_0$ but less) that more high fast-acting. Last, it is conditioned to those, that in such the ILE initial capacity of charge and runs down by the currents of the opened transistors.

Literature: [1, pp. 117–119]; [4, pp. 223–230]; [6]; [11]; [12]; [13]; [14].

2. EXECUTION OF THE WORK

The given laboratory work is executed by means plug-in card of a 8 “Research of dynamic parameters DIC”. An integral microcircuit K561LA7 is examined.

1. To familiarize with the electric circuit of the module (fig. 8.4) of principle, with disposing and setting of regulative elements on a panel. By means the potentiometer *R4* (on a panel marked U_{vh}) the state of circuit is set. In left extreme position on the gate of active transistor $U_{vh}^0 < U_0$ is set. Potentiometer E_C regulates voltage of source of feed from + 6 V(extreme left position) to + 9 V(extreme right position).

2. The dynamic parameters of digital microcircuits are measured by means the generator of rectangular pulses and dual-beam oscilloscope. An oscilloscope is connected thus: one entrance to the entrance 2 or directly to the generator, second entrance – to the output 4, corps – to the output 5. In the mode of external synchronization by means additional cable the output of synchronization of generator joins the entrance of synchronization of oscilloscope.

3. To include a stand, source of feed 12 V, generator and oscilloscope. Switches to translate ENTER of both channels on the front panel of oscilloscope in position “$\underline{\sim}$” (the entrance is opened, after a direct current). To translate a switch SYNCHRONIZATION in position ZOVN and pens LEVEL and STAB. to obtain proof synchronization by the pulses of generator (in case of setting off cable of synchronization from an oscilloscope the tracings must disappear).

4. To translate the handles of potentiometer U_{vh} in extreme left position, that is set on the entrances $U_{vh}^0 < U_0$. Thus on an output is set $U_{vuh}^1 = E_C$, that allows by

means the oscilloscope to measure voltage of source of feed. This voltage is proposed by a potentiometer U_{dzh}. It is necessary to propose at research of microcircuits K178LA7 or K561LA7 $E_{dzh} = 9\text{V}$. The trace of oscilloscope at the increase of voltage is displaced upwards. In screen of oscilloscope to mark levels $U_1 = 0$ and $U_2 = 9\text{V}$ (on a zero level the tracing is displaced either by disconnection of oscilloscope from an output 4, or by switching the ENTRANCE in position "~" (the entrance is closed, after an alternating current)).

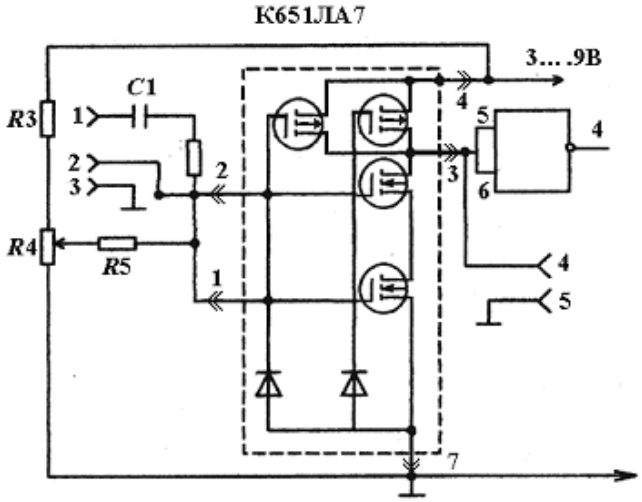


Fig. 8.4. Circuit of the laboratory module for research dynamic parameters DIC

5. To examine a circuit on implementation of logic function And – No:

– at extreme left position of potentiometer R4 to fix position of tracing of oscilloscope ($U^1_{vuh} = U_{dzh}$);

– by the rotation R4 clockwise to set on the entrance $U^1_{vh} > U_0$. Thus a circuit must pass to the opened state. The tracing of oscilloscope by a jump moves on a level which answers U^0_{vuh}.

To fix this level in protocol.

6. To define the threshold values of amplitude of impulsive signals which provide switched IC in the mode of cut off and in the mode of satiation:

– to connect the generator of rectangular pulses to the outputs 1 and 3. To set amplitude of pulses 2...4 V, duration 1 – 2 μs, frequency of reiteration – 100 kHz;

– to translate a circuit in the mode of cut off (U^1_{vuh}) by establishment of potentiometer R4 in extreme left position;

– to set positive polarity of initial pulses of generator and, multiplying their amplitude, to obtain appearance of negative pulses on an output. To fix the value of amplitude of entrance pulses and draw 2...4 oscillograph trace of output pulses in the range of considerable change of form of entrance pulses.

To transport a potentiometer R4 in right extreme position and give the pulses of negative polarity on the entrance.

To conduct research, as well as in previous case.

7. To measure duration of junction IC from the state of logical item in the state of logical zero ($t^{1,0}$), duration of junction IC from the state of logical zero in the state of logical item ($t^{0,1}$), duration of delay of including ($t^{1,0}_{delay}$), duration of delay of shutdown ($t^{0,1}_{delay}$), duration of delay of distribution at the inclusion ($t^{1,0}_{delay.distr}$), and shutdown ($t^{0,1}_{delay.distr}$). For this purpose:

– to translate a potentiometer R4 in extreme left position;

– to give on the entrances of integral microcircuit the pulses of positive polarity with the parameters mentioned higher; thus on the entrance the pulses of negative polarity must be formed. The channel of oscilloscope, which is connected to the entrance 2 reproduces the entrance pulses of positive polarity;

– by means the handles of oscilloscope after the first and second by channels to put together in screen an entrance and weekend the pulses. To set their size for vertical lines and time scale on a horizontal line (duration of tracing) such, that it was comfortably to execute measuring. By means the button and slow adjusting of delay on the front panel of generator it is possible to change position of pulse, that is examined, in relation to beginning of tracing in the mode of external synchronization (see p.3);

– to draw oscillograph trace of pulses in protocol, to measure the mentioned higher time intervals and inflict the got values on oscillograph trace (see fig. 8.1).

8. To define mean time of delay of distribution ILE.

9. To turn off measuring devices, sources of feed and stand.

10.To analyse the results. To formulate terminals and design protocol of the report.

3. CONTENTS OF THE REPORT

The report must contain:

1. The purpose of laboratory work.

2. The graphic image is conditional, electric circuit and dynamic parameters of the integrated circuit (K561LA7) of principle that is examined, taken from a reference book.

3. Circuit of the laboratory module for measuring of dynamic parameters dis.

4. Time diagrams of entrance and weekend of pulses (to specify the dynamic parameters got during experimental researches).

5. Results of researches, value of threshold voltage and dynamic parameters as tables and oscillograph trace.

4. QUIZ

1. Call basic dynamic parameters of logical IC.
2. What is the fast-acting IC limited to?
3. How do classify TSIS after the fast-acting?
4. Why has the emitter-linked logic the high fast-acting?
5. Draw the circuit of principle and account for principle of action of integral logical element on MOS-transistors with the dynamic loading.
6. How will boolean operation be realized And – NOT by means the CMOS-logic?
7. Compare after the fast-acting the logical elements executed on the MOS-transistor keys with the resistive load, with the dynamic loading and on KMOH-structures.
8. Why did junction from p-channel MOS-circuits to n- channel allow in 2–3 times to multiply the fast-acting DIC?
9. Name the performance parameters of digital IC.

BIBLIOGRAPHICAL REFERENCES

1. Medvedenko B. I. Elektronni priladi: Navch.posibnik. – K.: KMUTsA, 1999. – 168 s.
2. Rudenko V. S., Romashko V. Ya., Trifonyuk V. V. Promislova elektronIka: Pidruchnik. – K.: LibId, 1993. – 432 s.
3. Zherebtsov I. P. Osnovi elektroniki. – 5-e izd., pererob. i dop. – L.: Energoatomizdat, 1989. – 352 s.
4. Gershunskiy B. S. Osnovyi elektroniki i mikroelektroniki – 3-e izd. pererab. i dop. – Vischa shk., 1987. – 422 s.
5. Tranzistoryi dlya dlya apparaturyi shirokogo primenenya: Spravochnik /Pod red. B.L. Perelmana. – M.: Radio i svyaz, 1999. – 730 s.
6. Integralnyie mikroshemyi: Spravochnik /Pod red. B.V. Tarabrina. – M.: Radio i svyaz, 1984. – 528 s.
7. DSTU 2332-93 Diodi napivprovidnikovi. Termini, viznachennya, ta literni poznachennya elektrichnih parametriv.
8. DSTU 2307-93 Tranzistori bipolyarni. Termini, viznachennya ta literni poznachennya elektrichnih parametriv.
9. DSTU 2173-93 Tranzistori polovi. Termini, viznachennya ta literni poznachennya elektrichnih parametriv.
10. DSTU 2449-94 Priladi napivprovidnikovi. Termini ta viznachennya.
11. DSTU 2306-93 Mikroshemi Integralni. Termini ta viznachennya.
12. DSTU 2383-94 Mikroshemi Integralni. Termini, viznachennya ta literni poznachennya elektrichnih parametriv.
13. DSTU 3212-95 Mikroshemi Integralni. Klasifikatsiya ta sistema umovnih poznachen
14. Stepanenko I. P. Osnovyi mikroelektroniki. – M.: 1999. – 420 s.
15. Protasov A. Increasing of operation speed of digital eddy current defectoscopes based on frequency synthesizer / V. Bazhenov ; A. Protasov ; K. Gloinik // 2017 IEEE Microwaves, Radar and Remote Sensing Symposium (MRRS). Conf. proc. – Kyiv, Ukraine. – pp. 155-158.
16. Bazhenov V. Optimization of the algorithms for the work of eddy current flaw detectors on microcontrollers / V. Bazhenov; K. Gloinik; I. Lysenko // Scientific Proceedings, Bulgaria. – 2017. – Vol. 216 – pp. 118-120.